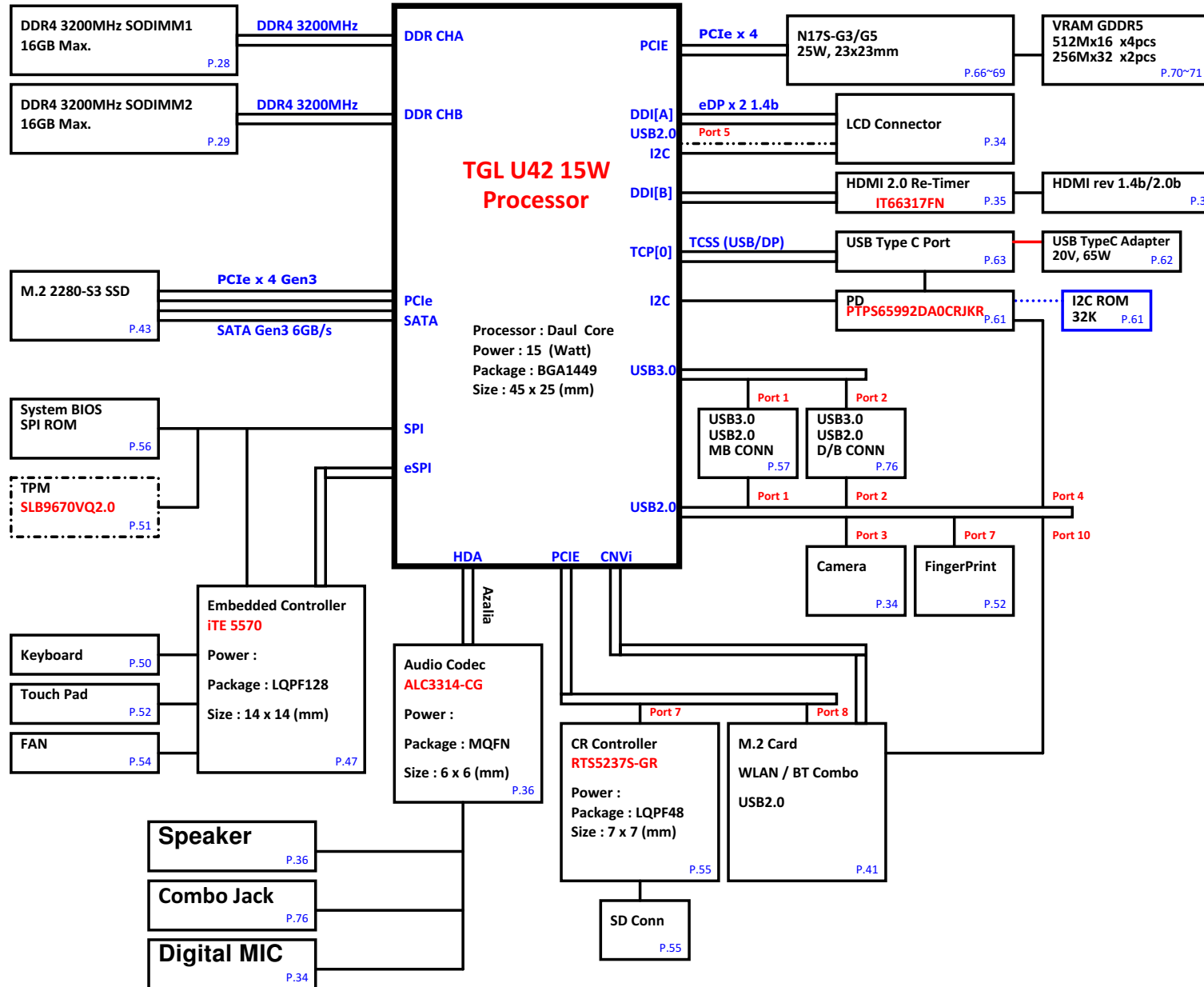


Space animal DIS/UMA 15.6"

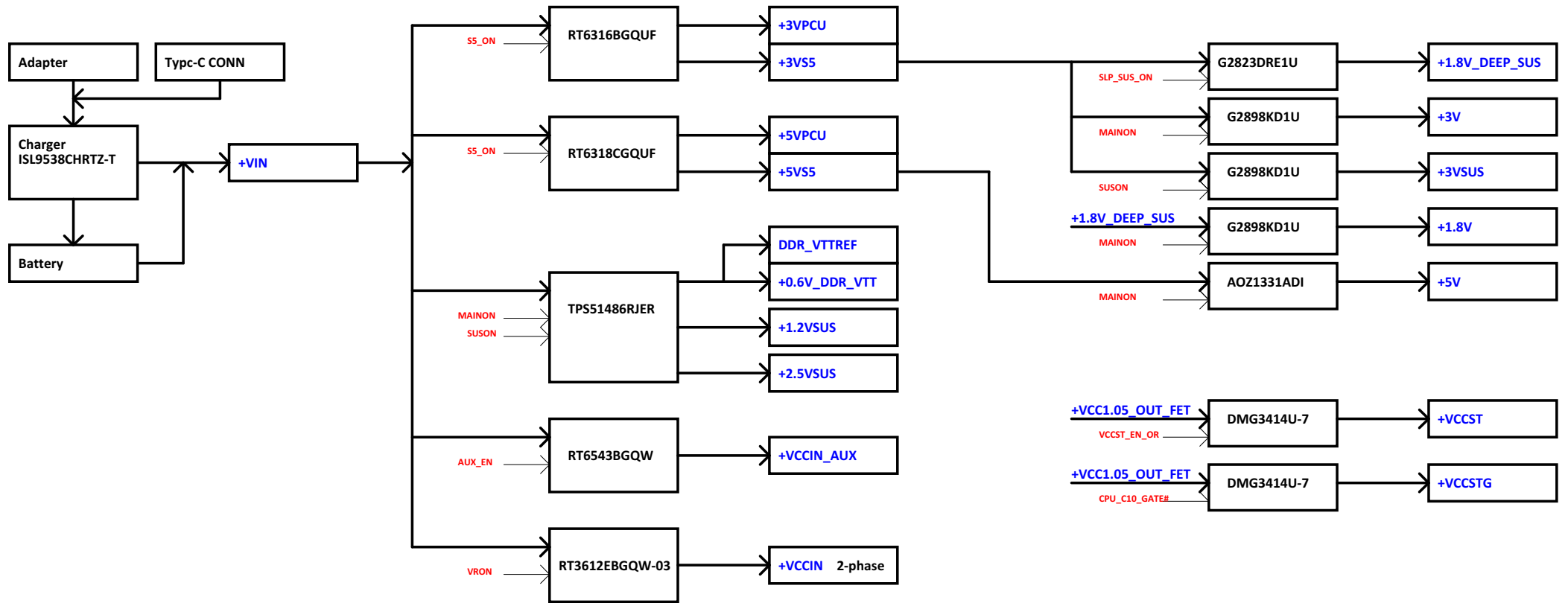
Intel TGL U42 Platform Block Diagram

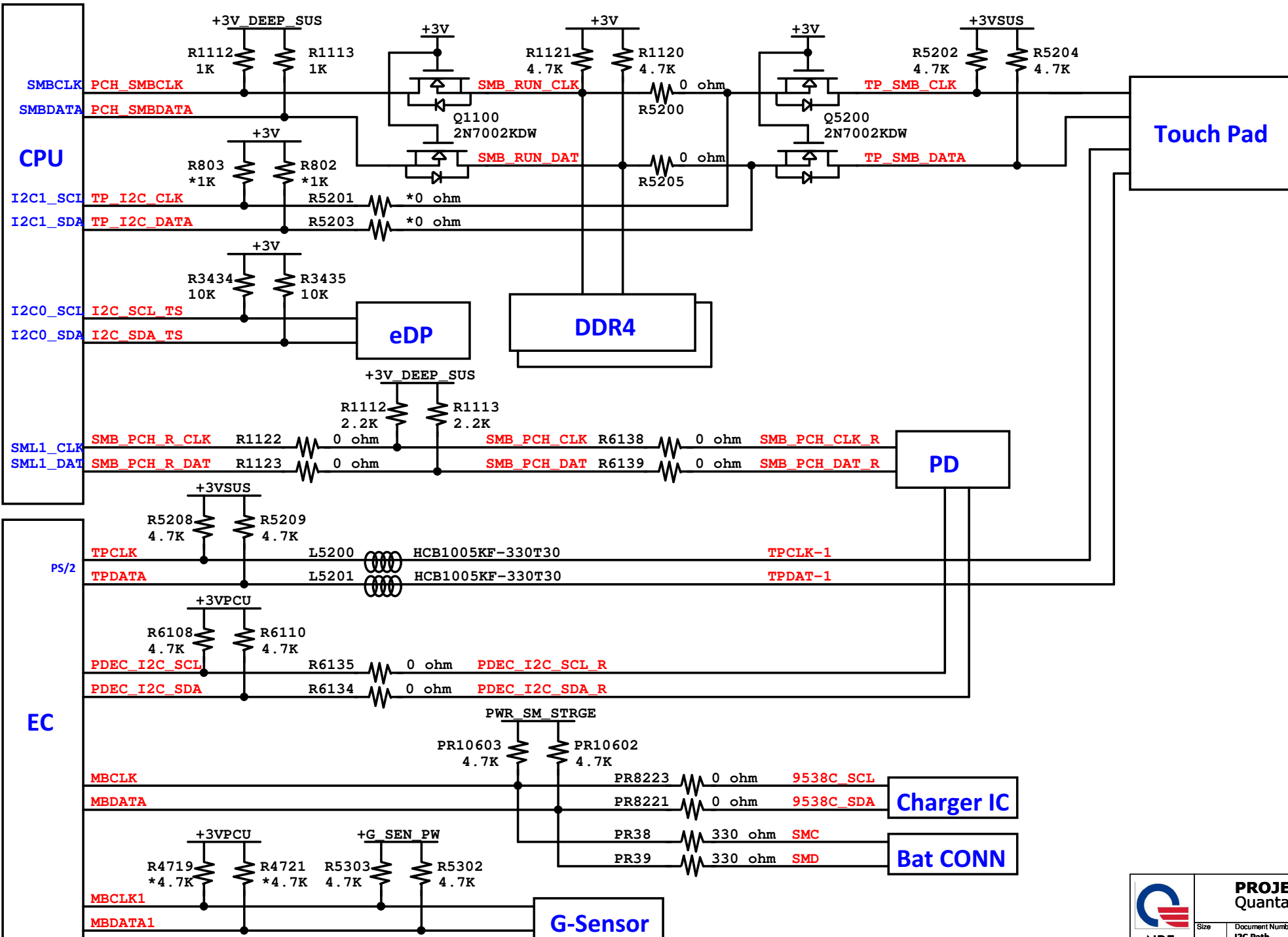
01



PCB 8L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : IN3
 LAYER 7 : SGND1
 LAYER 8 : BOT





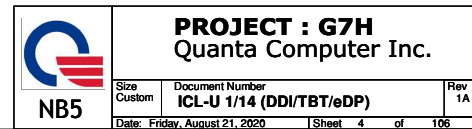


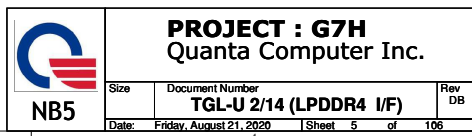
Johnny's

+3V DEEP SUS

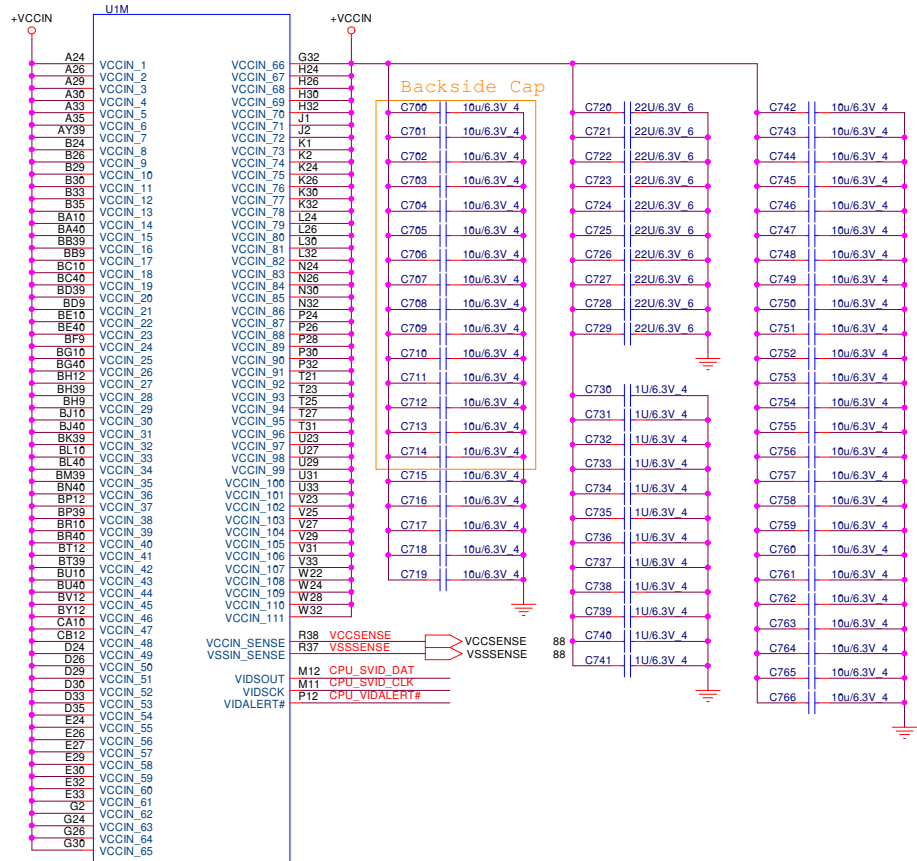
R404 10K 5% 2 USB_OC1#
R405 10K 5% 2 USB_OC2#

strap pin

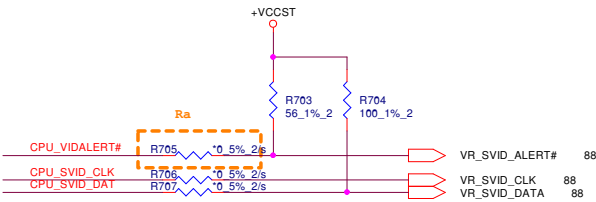
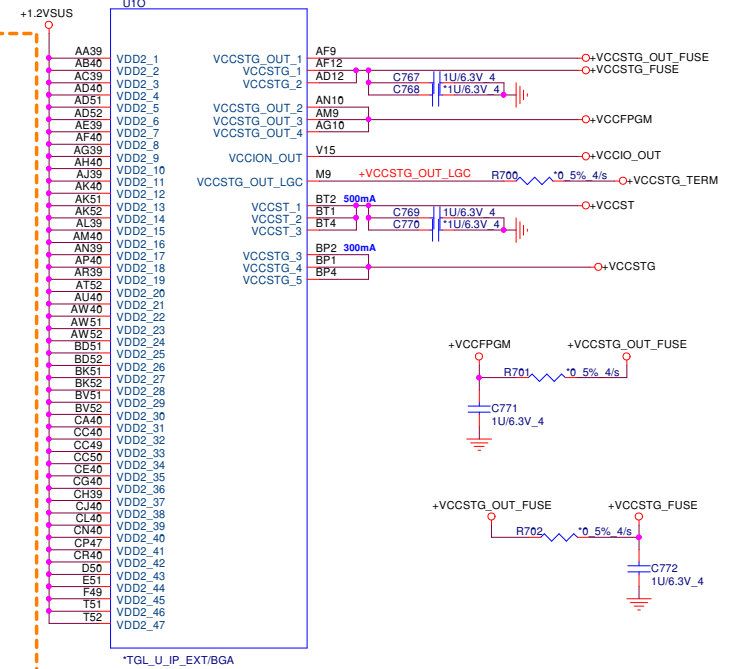
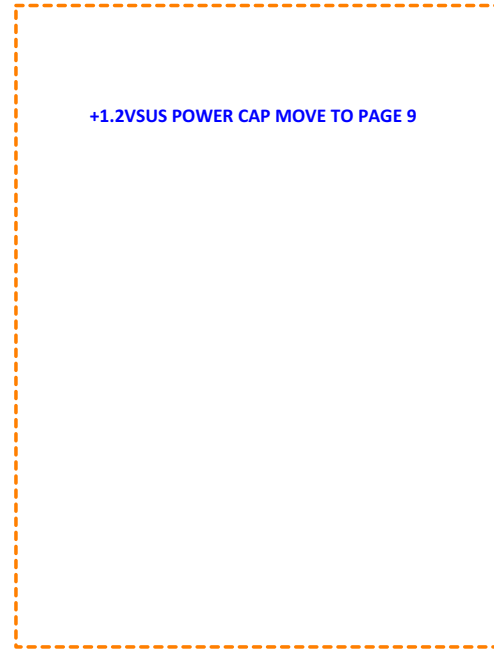




+VCCIN: 65A



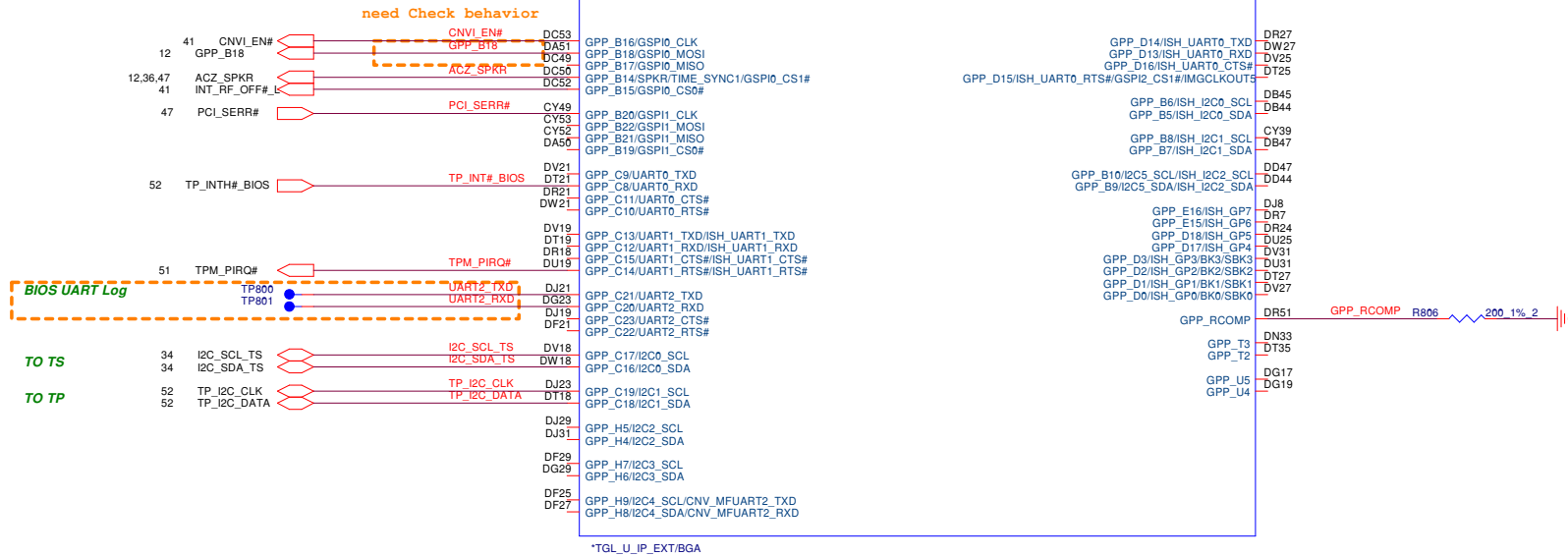
+1.2VSUS: 1.5A

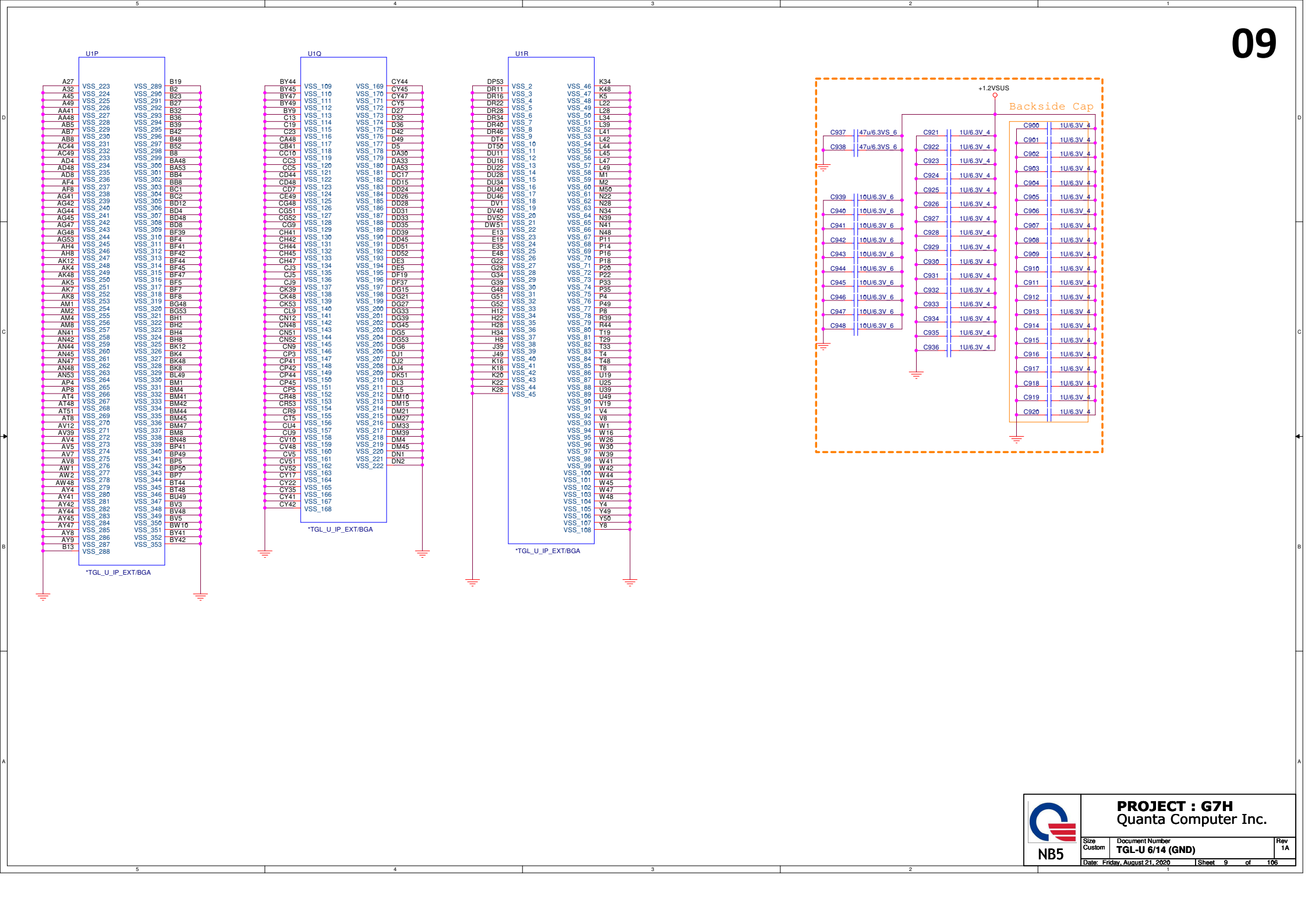


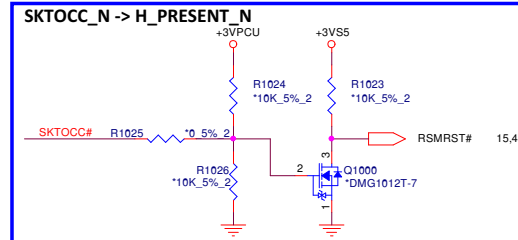
ALERT# needs to Place between CLK and DAT
Ra Neen check value

01/17 Add SOC_ENBKL for S5 Turn off
the Backlight

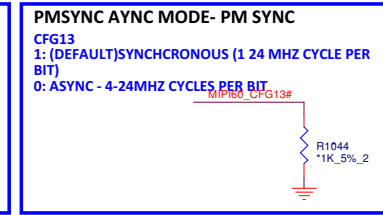
CNVI_EN# PD 75K @ WLAN side
need Check with BIOS







PROC_SELECT




NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG9

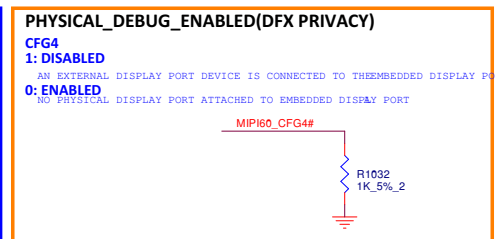
1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT

0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP
WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY



MIP160_CFG9#

R1033
1K_5%_2



PEG DEFER TRAINING

CFG7


1: (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB
DEASSERTION

0: PEG WAIT FOR BIOS FOR TRAINING

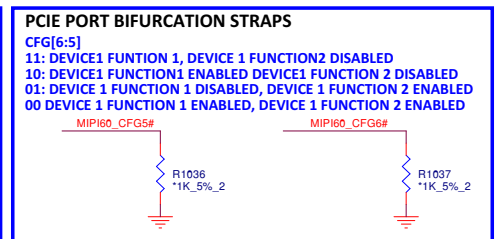
The diagram shows a circuit connection for the MIPi60_CFG7# signal. A horizontal line representing the signal trace is connected to a vertical line. This vertical line passes through a resistor, represented by a zigzag symbol. To the right of the resistor, the text 'R1031' and '*1K_5%_2' are present. The bottom of the resistor is connected to a ground symbol, which consists of three horizontal lines of decreasing width.

SAFE MODE BOOT

CFG10
1: POWER FEATURES ACTIVATED DURING RESET
0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED



The diagram shows a red line representing the MIP160_CFG10# signal pin. This pin is connected to a resistor labeled R1039, which has a value of 1K 5% 2. The other end of the resistor is connected to a ground symbol, represented by three horizontal lines of decreasing width.



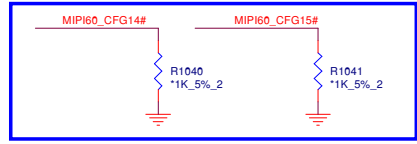
ALLOW THE USE OF NOA ON LOCKED UNITS

CFG8

1: DISABLED(DEFAULT): IN THHIS CASE, NOA WILL BE
DISABLE IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS

0: ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF
THE LOCKING OF THE UNIT

The diagram shows a red line representing a signal trace for the pin MIP160_CFG8#. This line passes through a resistor, labeled R1038 with a value of 1K_5%_2, and then connects to a ground symbol. The ground symbol consists of three horizontal lines of decreasing width, representing a connection to the system ground.

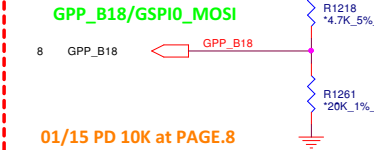


TOP SWAP OVERRIDE

High: TOP SWAP ENABLED
Low: DISABLED
WEAK INTERNAL PD 20K

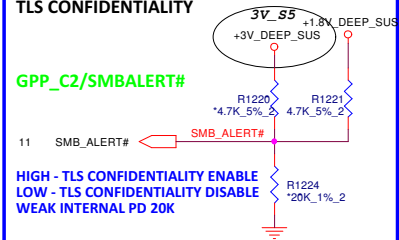
**NO REBOOT**

High: NO REBOOT
Low: REBOOT ENABLED
WEAK INTERNAL PD 20K

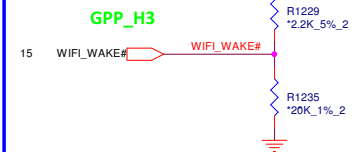
**TLS CONFIDENTIALITY**

GPP_C2/SMBALERT#

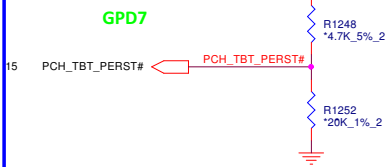
High - TLS CONFIDENTIALITY ENABLE
Low - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K

**MAF/SAF STRAP**

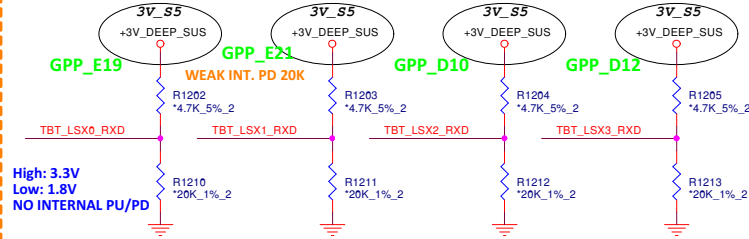
High: SAF ENABLE
Low: MAF ENABLE
WEAK INTERNAL PD 20K

**(RSVD) XTAL INPUT MODE**

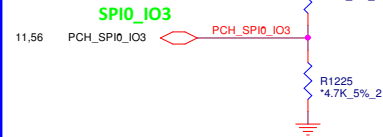
High: XTAL INPUT IS SINGLE ENDED
Low: XTAL IS ATTACHED
WEAK INTERNAL PD 20K

**TBT LSX PINS VCCIO CONFIGURATION**

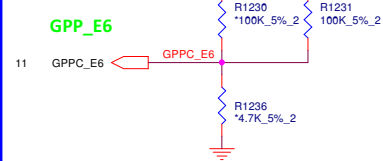
High: 3.3V
Low: 1.8V
NO INTERNAL PU/PD

**(RSVD) A0 PERSONALITY STRAP**

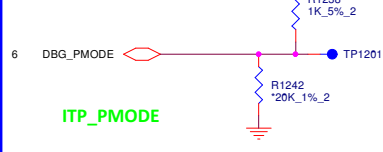
High: DISABLE
Low: ENABLE
External pull-up is required.

**(RSVD) JTAG ODT DISABLE**

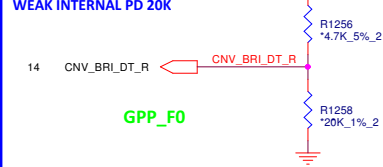
High: JTAG ODT Enable
Low: JTAG ODT Disable
External pull-up is required.

**(RSVD) ITP PMODE**

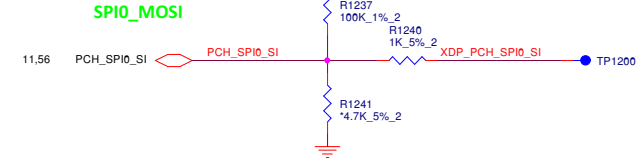
High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K

**XTAL FREQUENCY SEL**

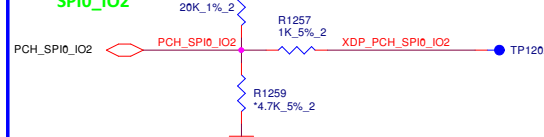
High: 24MHZ
(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
Low: 38.4MHZ (DEFAULT)
WEAK INTERNAL PD 20K

**(RSVD) BOOT HALT**

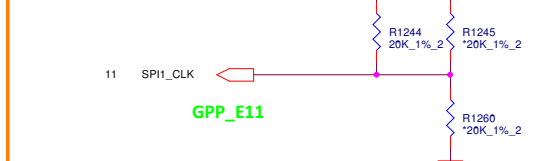
High: DISABLE
Low: ENABLE
External pull-up is required.

**(RSVD) CONSENT STRAP**

High: DISABLE
Low: ENABLE
External pull-up is required.

**THC0_SPI1_CLK**

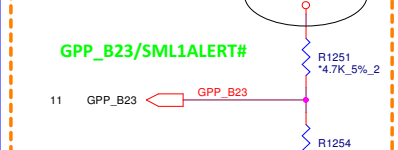
THC0_SPI1 Clock: THC SPI1 clock output from PCH. Supports 20 MHz, 33 MHz and 50 MHz.

**THC0_SPI1_CS#**

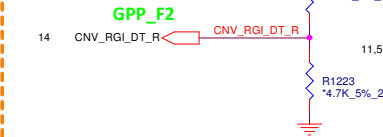
THC0_SPI1 Chip Select: Used to select the touch devices if it is connected to THC0_SPI1 interface.

**CPUNSSC CLOCK FREQ**

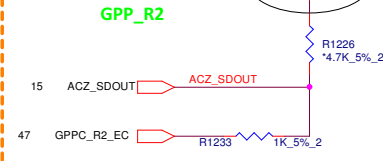
High: 19.2MHz CLOCK FROM INTERNAL DIVIDER
Low: 38.4MHz CLOCK FROM DIRECT CRYSTAL (Default)
WEAK INTERNAL PD 20K

**M.2 CNVi Mode Select**

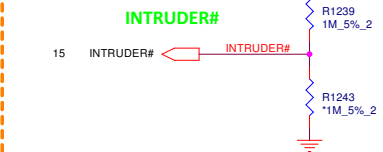
High: Integrated CNVi disabled
Low: Integrated CNVi enabled
An external pull-up or pull-down is required

**Flash Descriptor Security Override**

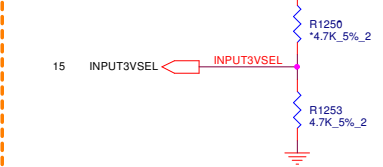
High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K

**Reduce leakage from Coin Cell Batt**

High: ENABLE
Low: DISABLE

**3V SELECT STRAP**

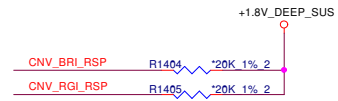
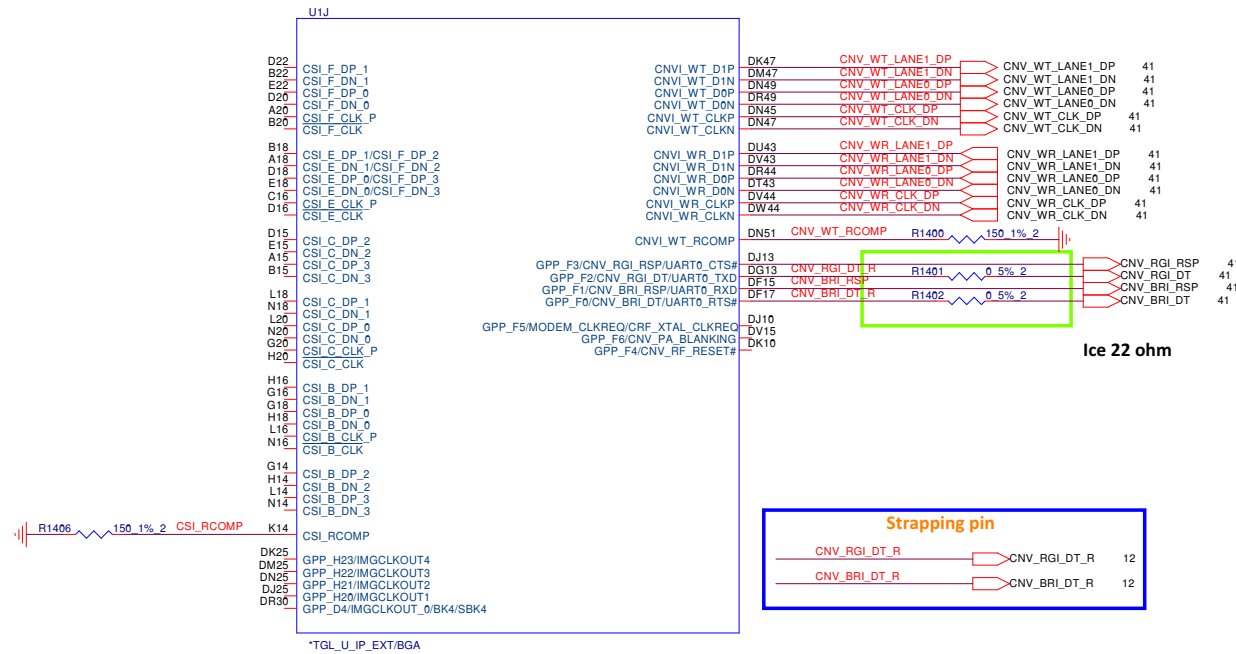
0 = SPI voltage is 3.3V (4.7K ohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K ohm pull-up to DSW_PWROK)



Because page size limited, some strap pin move to page 17

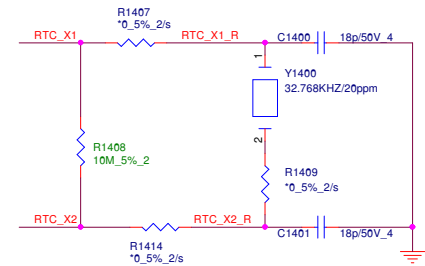


Size Custom	Document Number TGL-U 10/14(USB/PCIE/SAT)	Rev 1A
Date: Friday, August 21, 2020		Sheet 13 of 106

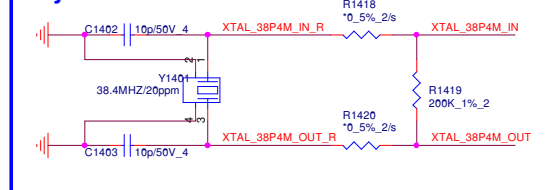


Crystal Components with Surrounding 10 mil Wide GNDshield Trace
Break Out:4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz



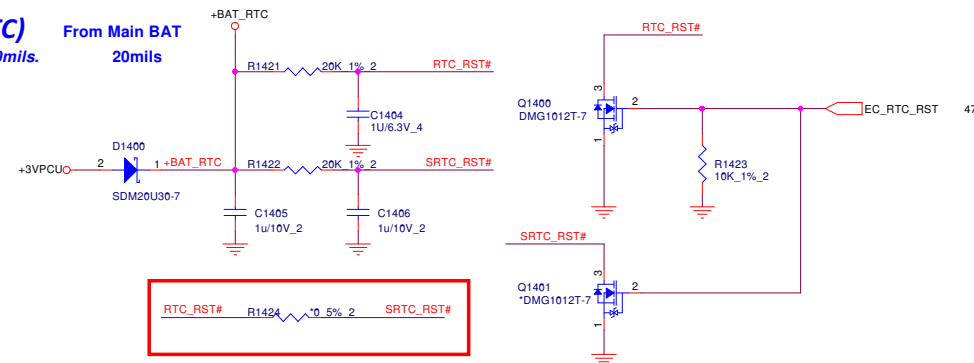
Crystal 38.4MHz

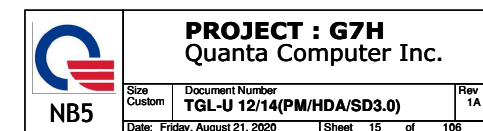
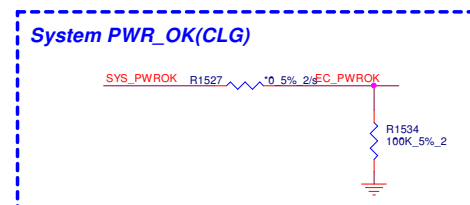
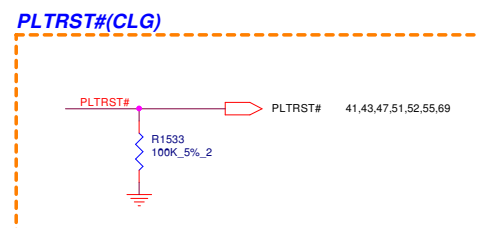
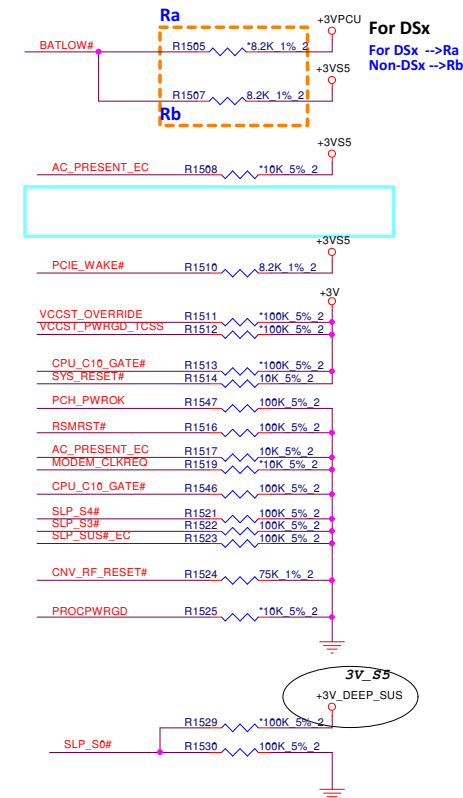


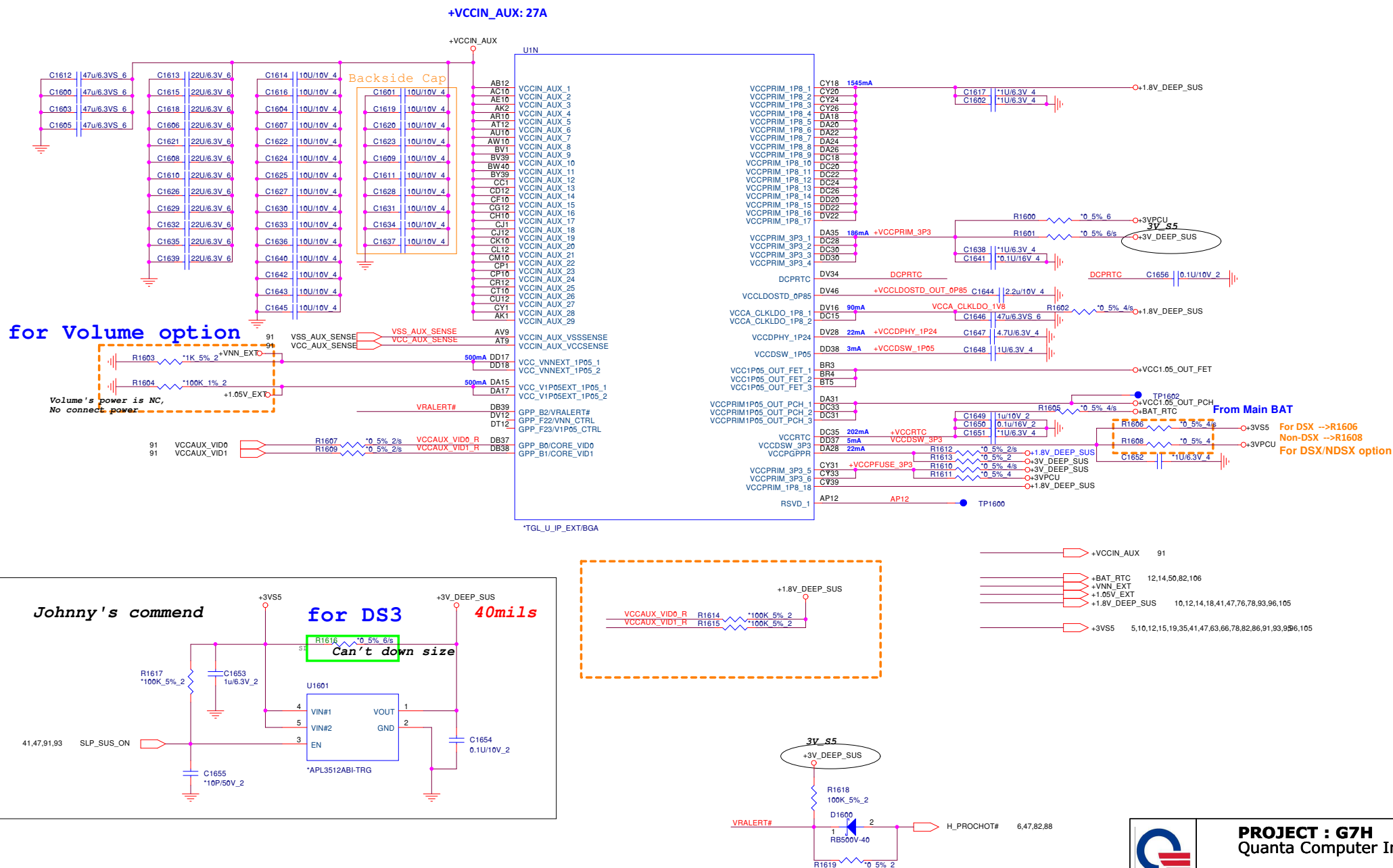
RTC Circuitry(RTC)

RTC Power trace width 20mils.

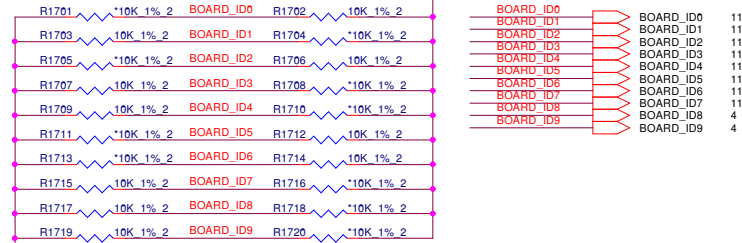
From Main BAT
20mils



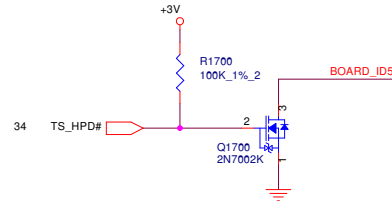




+3V_DEEP_SUS



For Touch screen Determination



+3V 6,8,11,12,13,14,15,21,28,29,34,35,43,47,50,52,56,59,82,88,96,98,102
+3VS5 5,10,12,15,16,19,35,41,47,63,66,78,82,86,91,93,95,96,105
+3V_DEEP_SUS 4,11,12,13,15,16,50,56,61

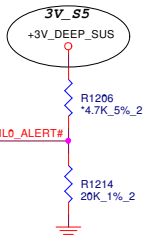
Model	BOARD_ID[9:7]	BOARD_ID6	Board ID5	Board ID4	BOARD_ID[3:1]	BOARD_ID0
GoT ICE	MD Sku only 000:Samsung 001:Hynix 010:Micron 100:Sam 16G K4AAG165WB-MCRC 110:Sam 16G K4AAG165WB-MCTD 111:XXX	0: N17S 1: N18S	0: Non-I2C TS 1: I2C TS active by LCD cable	0: VRAM 2G 1: VRAM 4G	000: Able 001:Dezik 010:Strelka	0: UMA 1: DIS

Boot Strap 0

WEAK INTERNAL PD 20K

GPP_C5/SMLOALERT#

11 SML0_ALERT#

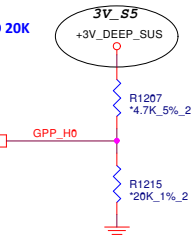


Boot Strap 1

WEAK INTERNAL PD 20K

GPP_H0

6 GPP_H0

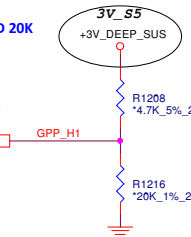


Boot Strap 2

WEAK INTERNAL PD 20K

GPP_H1

6 GPP_H1

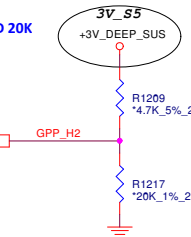


Boot Strap 3

WEAK INTERNAL PD 20K

GPP_H2

6 GPP_H2



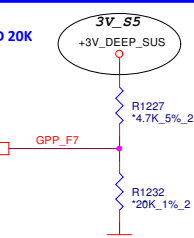
Boot Strap	4-bit boot strap configuration encodings
0000	BIOS/CSME on SPI & eSPI is enabled
0010	BIOS/CSME on SPI & eSPI is disabled
0100	BIOS on eSPI Peripheral Channel; CSME on master SP
1000	BIOS/CSME on eSPI
1100	BIOS on eSPI peripheral Channel; CSME on slave SPI

Reserved

WEAK INTERNAL PD 20K

GPP_F7

6 GPP_F7

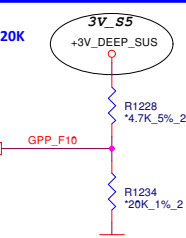


Reserved

WEAK INTERNAL PD 20K

GPP_F10

6 GPP_F10



RING OSCILLATOR BYPASS

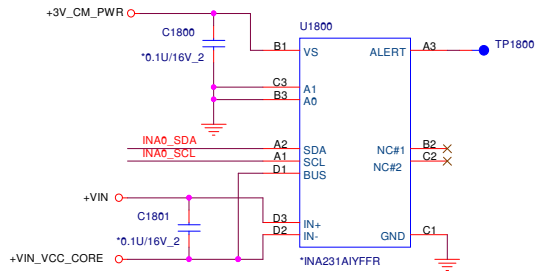
High: BYPASS MODE ENABLED
Low: RING OSCILLATOR
(QUALIFIED BY DFTESTMODE)
NO INTERNAL PU/PD

GPP_H3

+VCCIN

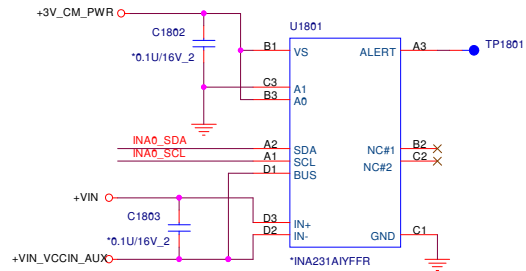
Slave Addresses:1000000 Placed close to PR8708

INA0_SCL/SDA

**+VCCIN_AUX**

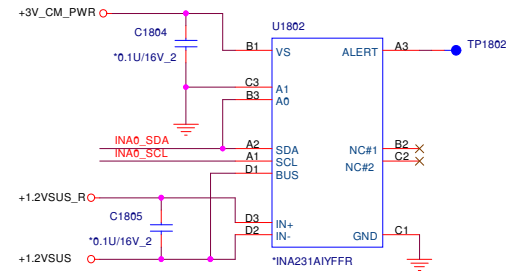
Slave Addresses:1000001 Placed close to PR9204

INA0_SCL/SDA

**+1.2VSUS**

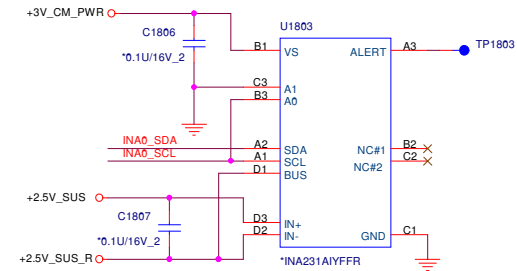
Slave Addresses:1000010 Placed close to PR8705

INA0_SCL/SDA

**+2.5V_SUS**

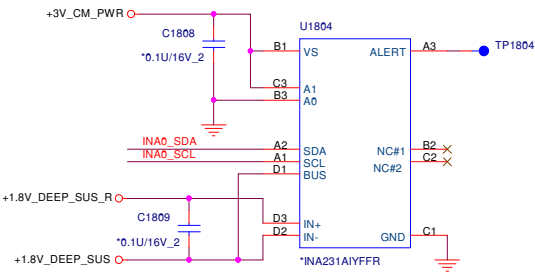
Slave Addresses:1000011 Placed close to PR8701

INA0_SCL/SDA

**+1.8V_DEEP_SUS**

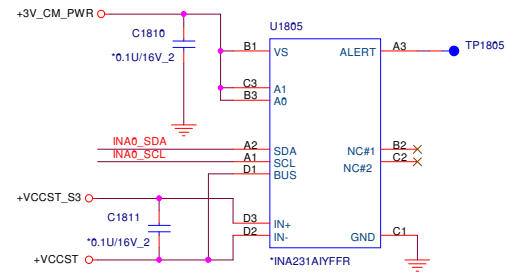
Slave Addresses:1000100 Placed close to PR9302

INA0_SCL/SDA

**+VCCST**

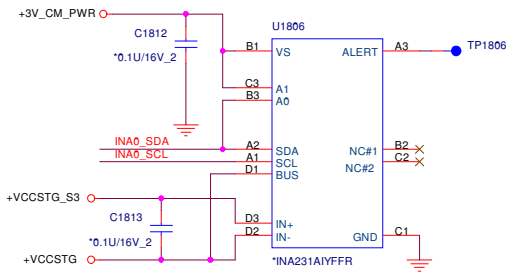
Slave Addresses:1000101

INA0_SCL/SDA

**+VCCSTG**

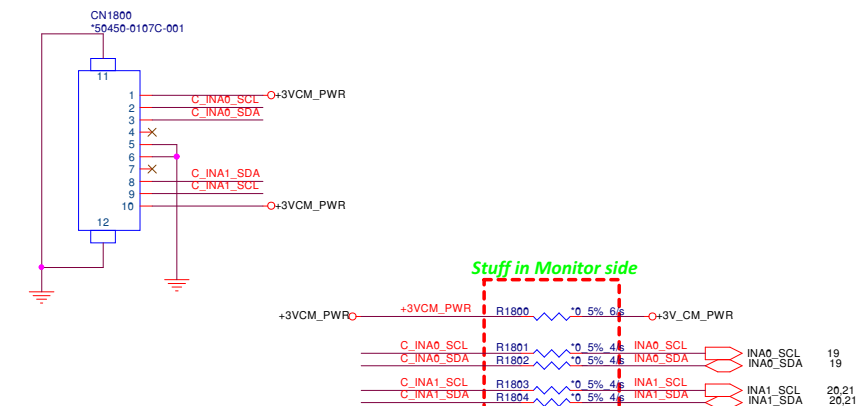
Slave Addresses:1000110

INA0_SCL/SDA

**+VAD**

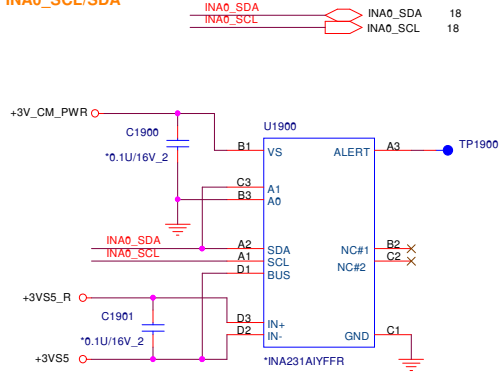
Slave Addresses:1000111 Placed close to PR8201

INA0_SCL/SDA

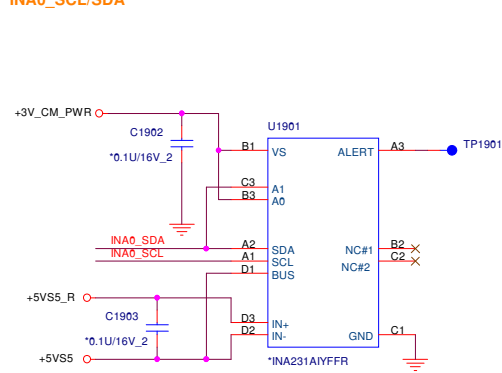
**Table 7. INA231 Address Pins and Slave Addresses**

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V _S	1000001
GND	SDA	1000010
GND	SCL	1000011
V _S	GND	1000100
V _S	V _S	1000101
V _S	SDA	1000110
V _S	SCL	1000111
SDA	GND	1001000
SDA	V _S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _S	1001101
SCL	SDA	1001110
SCL	SCL	1001111

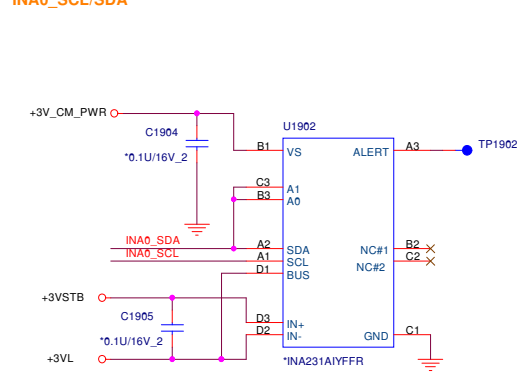
+3VS5
Slave Addresses:1001000 Placed close to PR8604
INA0_SCL/SDA



+5VS5
Slave Addresses:1001001 Placed close to PR8618
INA0_SCL/SDA



EC
Slave Addresses:1001010 Placed close to L4704
INA0_SCL/SDA



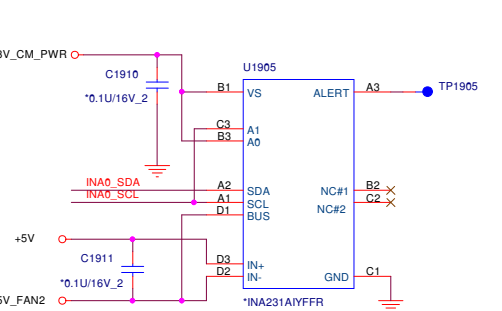
Battery (DC mode)
Slave Addresses:1001011 Placed close to PR8200
INA0_SCL/SDA

19

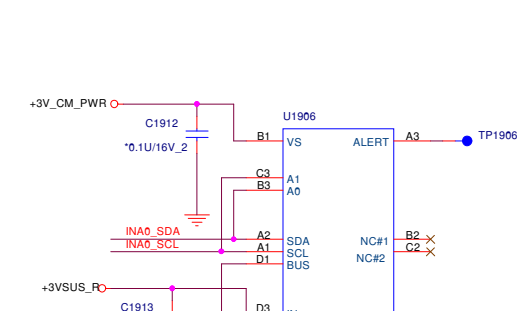
Slave Addresses:1001100 Placed close to PR9601
INA0_SCL/SDA



FAN2
Slave Addresses:1001101 Placed close to PR9602
INA0_SCL/SDA



+3VSUS
Slave Addresses:1001110 Placed close to PR9600
INA0_SCL/SDA

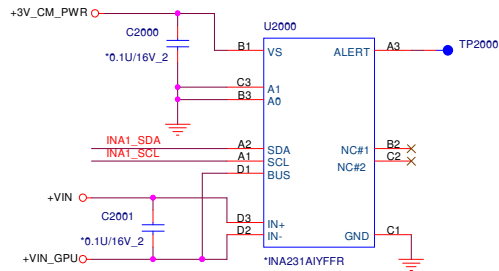


+1.8V
Slave Addresses:1001111 Placed close to PR9608
INA0_SCL/SDA

NVDD

Slave Addresses:100000 Placed close to PR9802

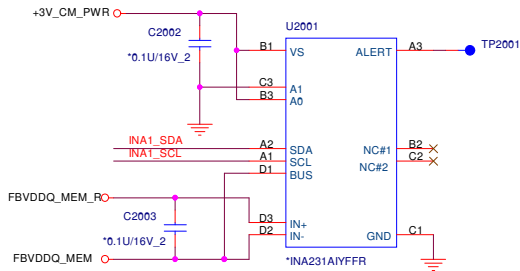
INA1_SCL/SDA



FBVDDQ_MEM

Slave Addresses:1000001 Placed close to PR10203

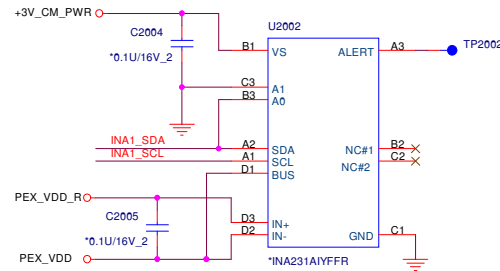
INA1_SCL/SDA



PEX_VDD

Slave Addresses:1000010 Placed close to PR10505

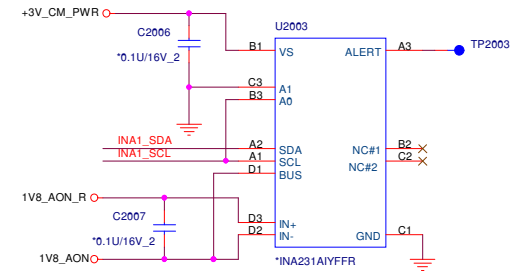
INA1_SCL/SDA



1V8_AON

Slave Addresses:1000011 Placed close to PR10514

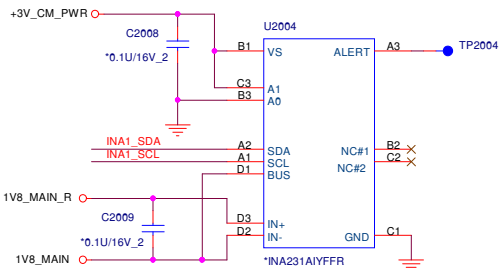
INA1_SCL/SDA



1V8_MAIN

Slave Addresses:1000100 Placed close to PR10513

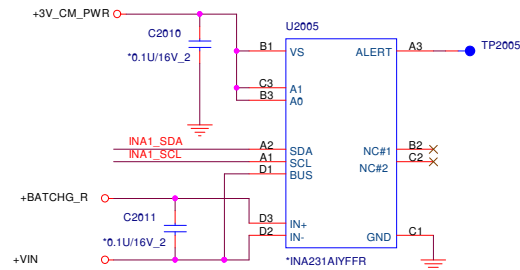
INA1_SCL/SDA



Battery

Slave Addresses:1000101 Placed close to L3407

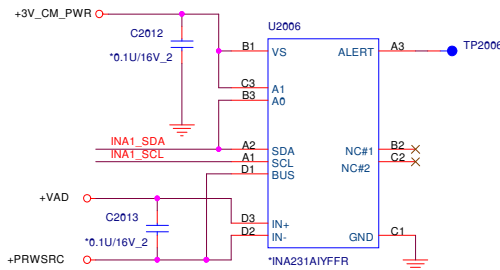
INA1_SCL/SDA



charge

Slave Addresses:1000110 Placed close to L3406

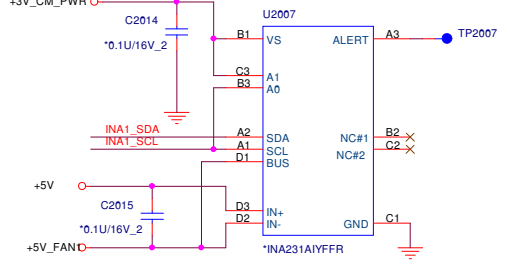
INA1_SCL/SDA



FAN1

Slave Addresses:1000111 Placed close to R3433

INA1_SCL/SDA



WLAN

Slave Addresses:1001000 Placed close to R4128

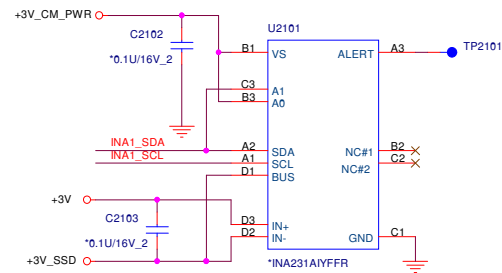
INA1_SCL/SDA



SSD

Slave Addresses:1001001 Placed close to R4300

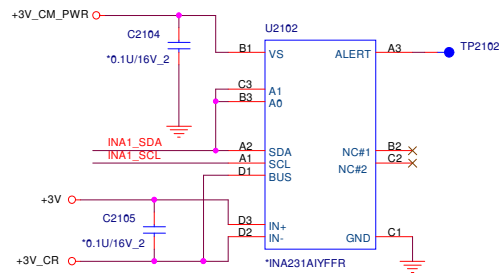
INA1_SCL/SDA



Card Reader

Slave Addresses:1001010 Placed close to R5500

INA1_SCL/SDA



SPI ROM

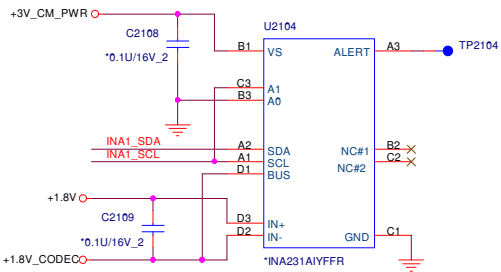
Slave Addresses:1001011 Placed close to R5621

INA1_SCL/SDA

Codec +1.8V

Slave Addresses:1001100 Placed close to R3616

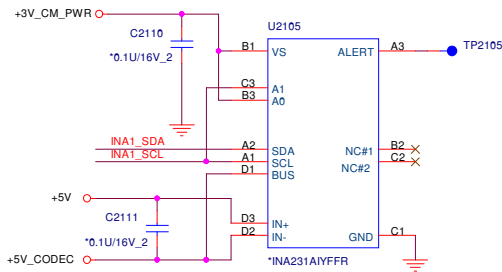
INA1_SCL/SDA



Codec +5V

Slave Addresses:1001101 Placed close to R3617

INA1_SCL/SDA



CAMERA

Slave Addresses:1001110 Placed close to R3434

INA1_SCL/SDA

IR CAM PWR

Slave Addresses:1001111 Placed close to R3435

INA1_SCL/SDA

PD
Slave Addresses:1000000 Placed close to R6131
INB0_SCL/SDA

PD_ROM
Slave Addresses:1000001 Placed close to R6100
INB0_SCL/SDA

FAN1
Slave Addresses:1000010 Placed close to R5402
INB0_SCL/SDA

FAN2
Slave Addresses:1000011 Placed close to R5403
INB0_SCL/SDA

Finger Print
Slave Addresses:1000100 Placed close to R5225
INB0_SCL/SDA

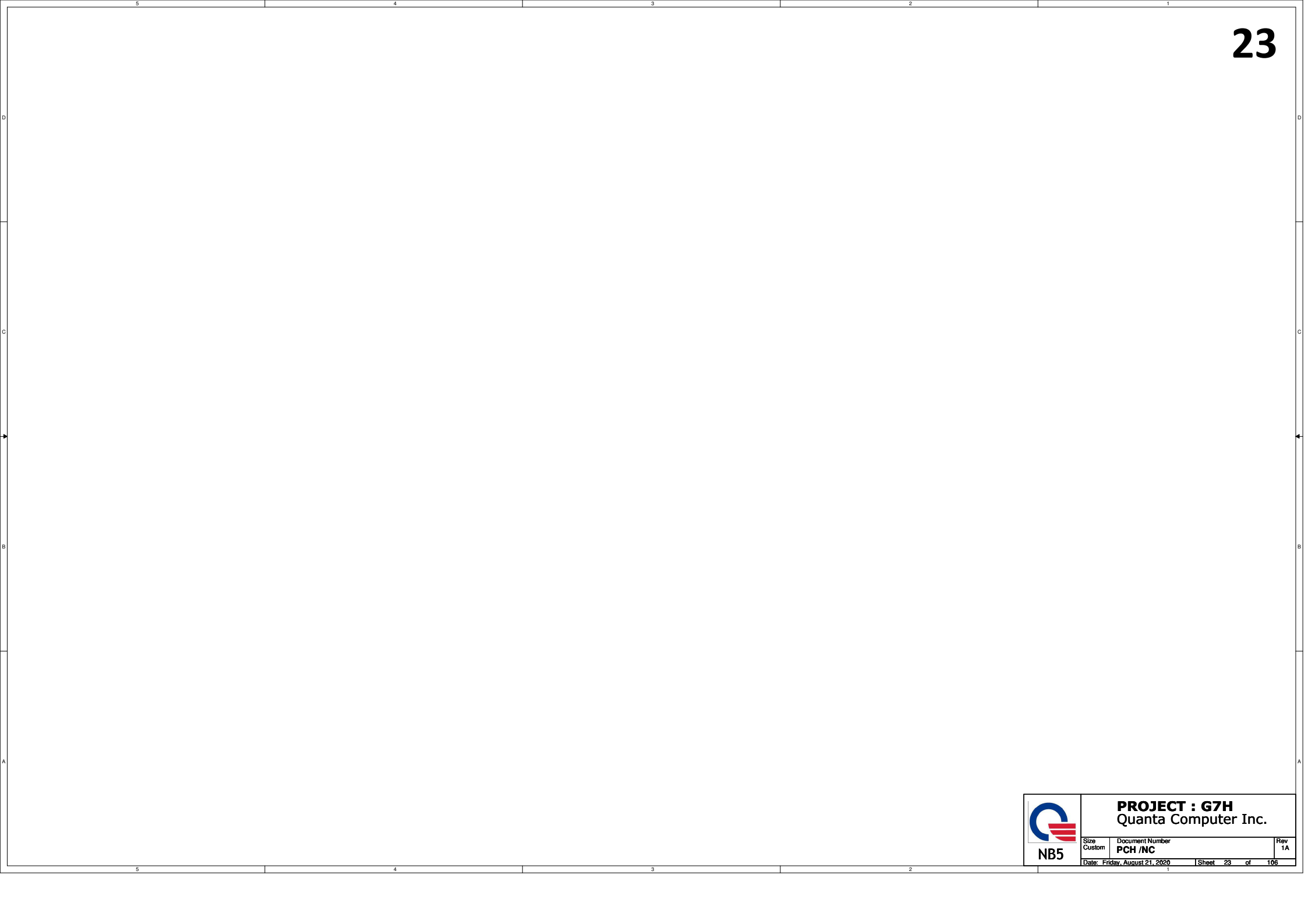
TPM
Slave Addresses:1000101 Placed close to R5100
INB0_SCL/SDA


TBD
Slave Addresses:1000110 Placed close to
INB0_SCL/SDA


TBD
Slave Addresses:1000111 Placed close to
INB0_SCL/SDA

Table 7. INA231 Address Pins and Slave Addresses

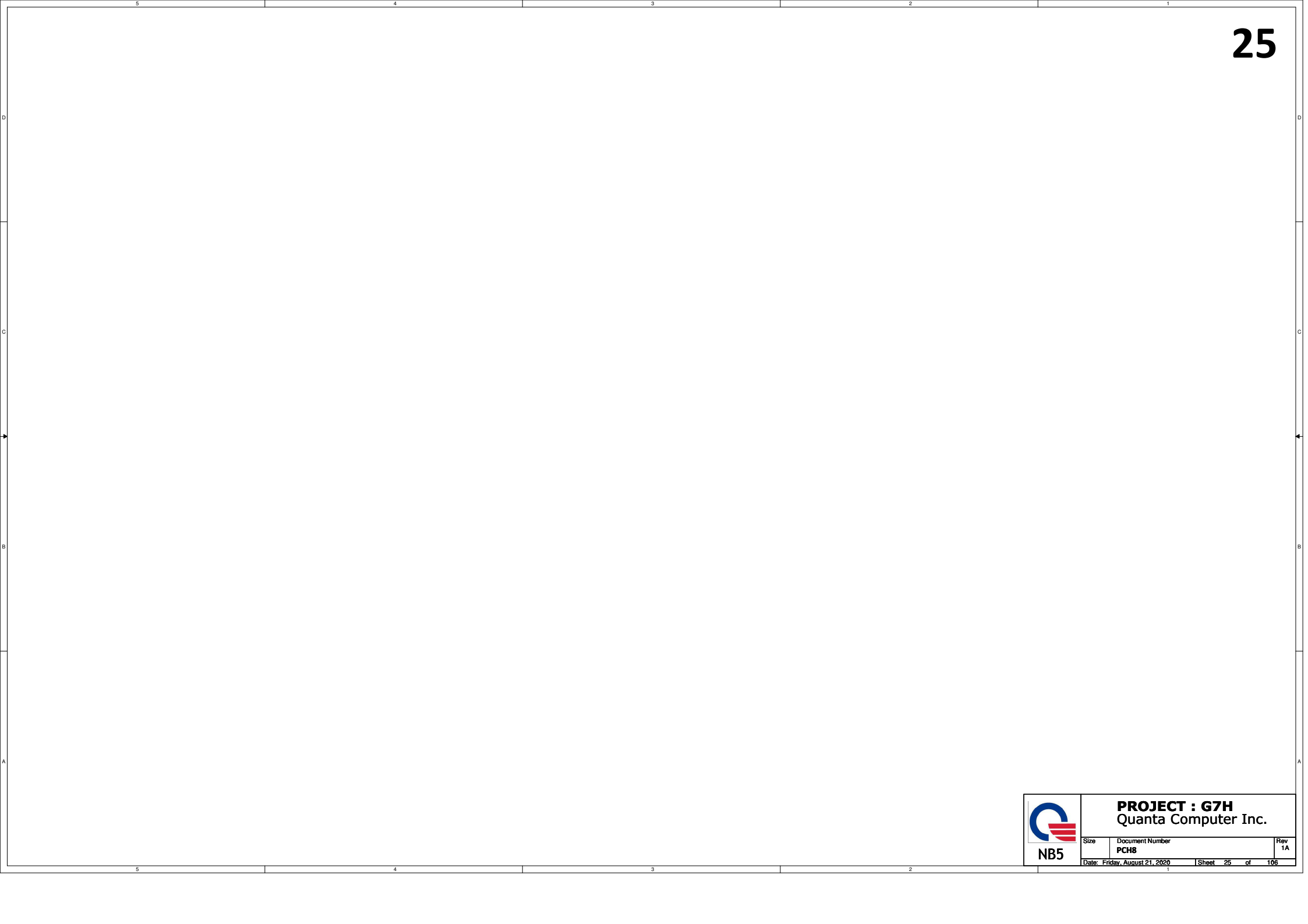
A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V _S	1000001
GND	SDA	1000010
GND	SCL	1000011
V _S	GND	1000100
V _S	V _S	1000101
V _S	SDA	1000110
V _S	SCL	1000111
SDA	GND	1001000
SDA	V _S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _S	1001101
SCL	SDA	1001110
SCL	SCL	1001111




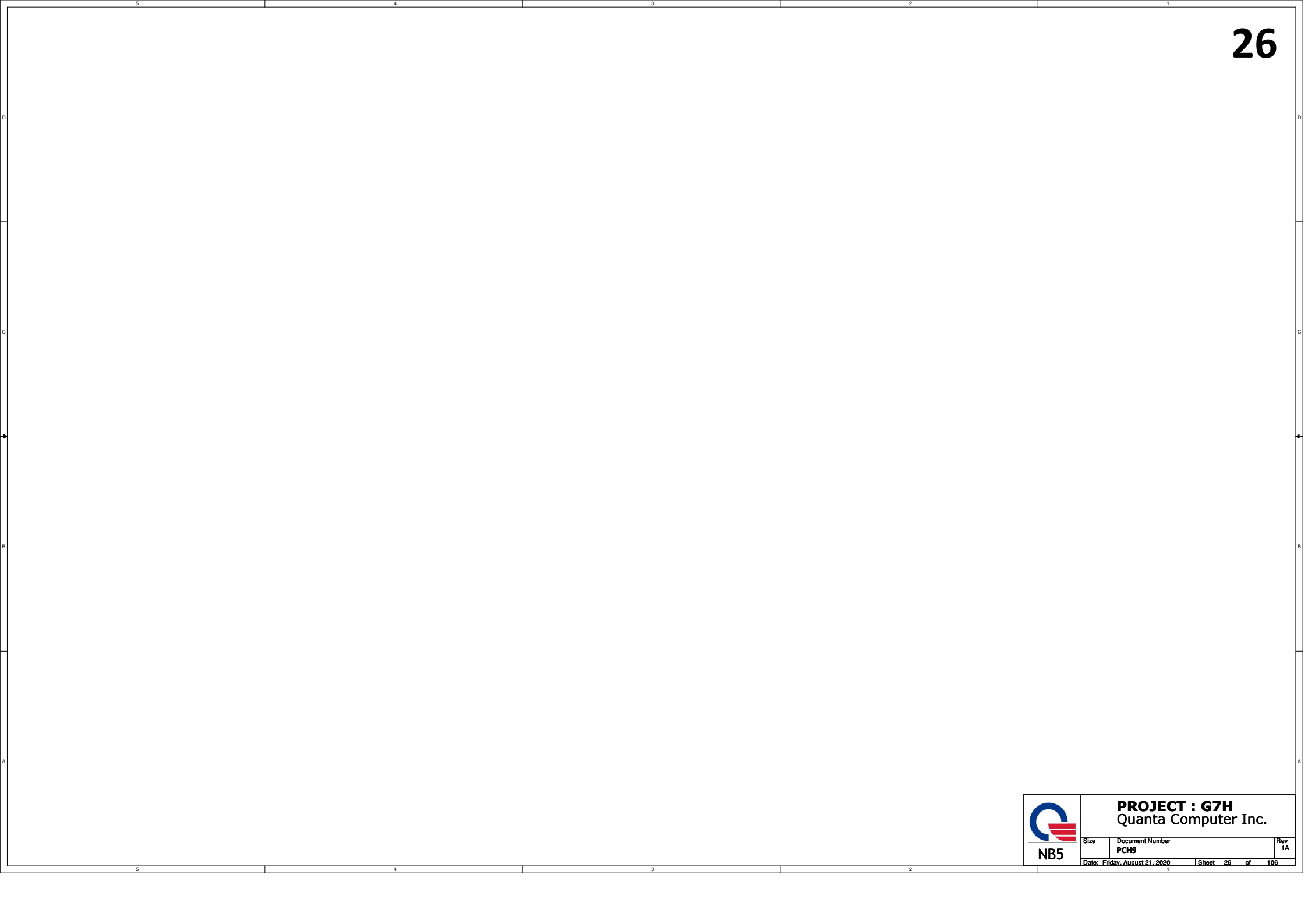
	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number PCH /NC	Rev 1A
	Date: Friday, August 21, 2020 Sheet 23 of 106		


 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number PCH /NC	Rev 1A
	Date: Friday, August 21, 2020		


Sheet 24 of 106

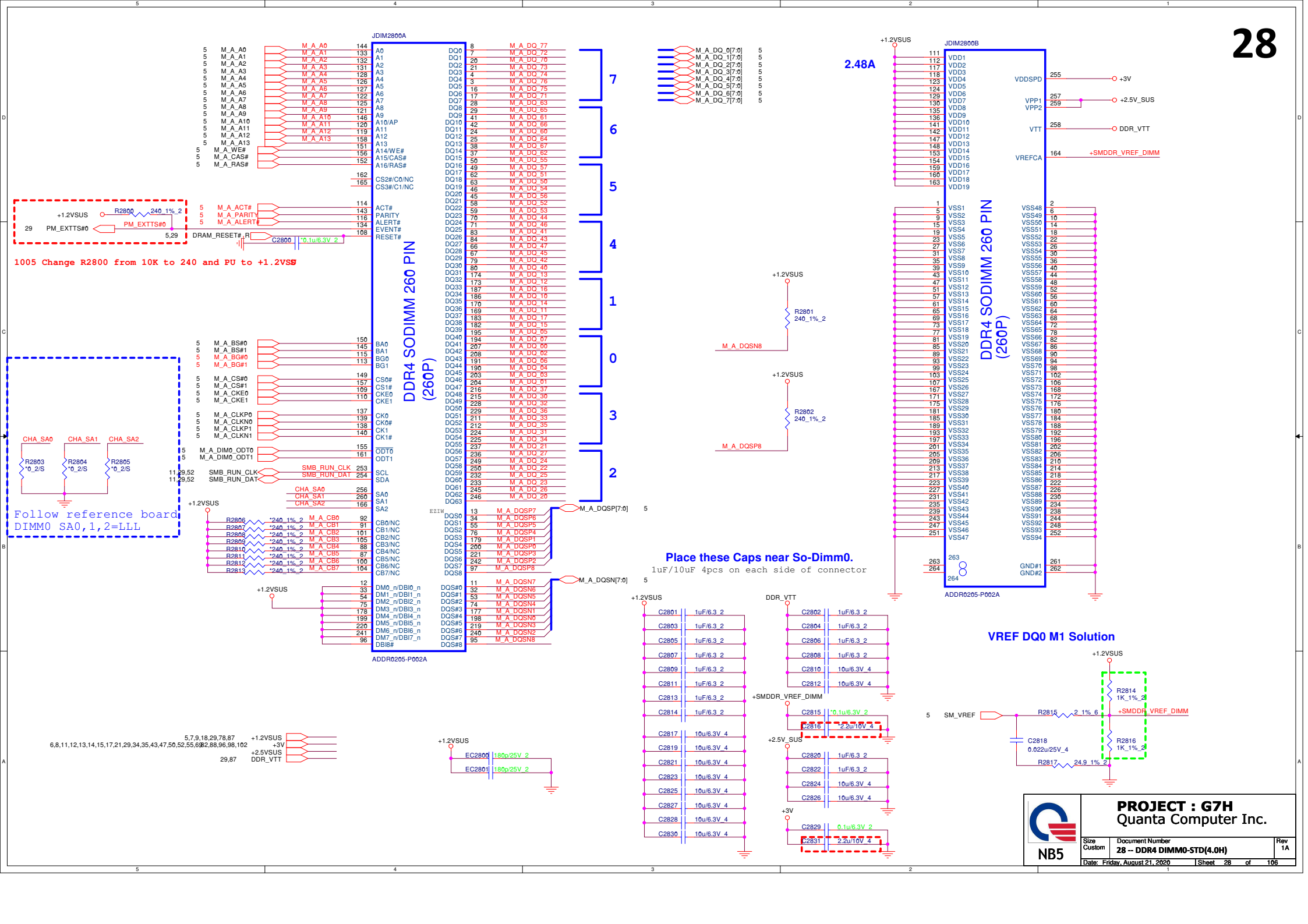


	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		PCH8	1A
Date: Friday, August 21, 2020 Sheet 25 of 106			





 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		PCH9	1A
Date: Friday, August 21, 2020 Sheet 26 of 106			

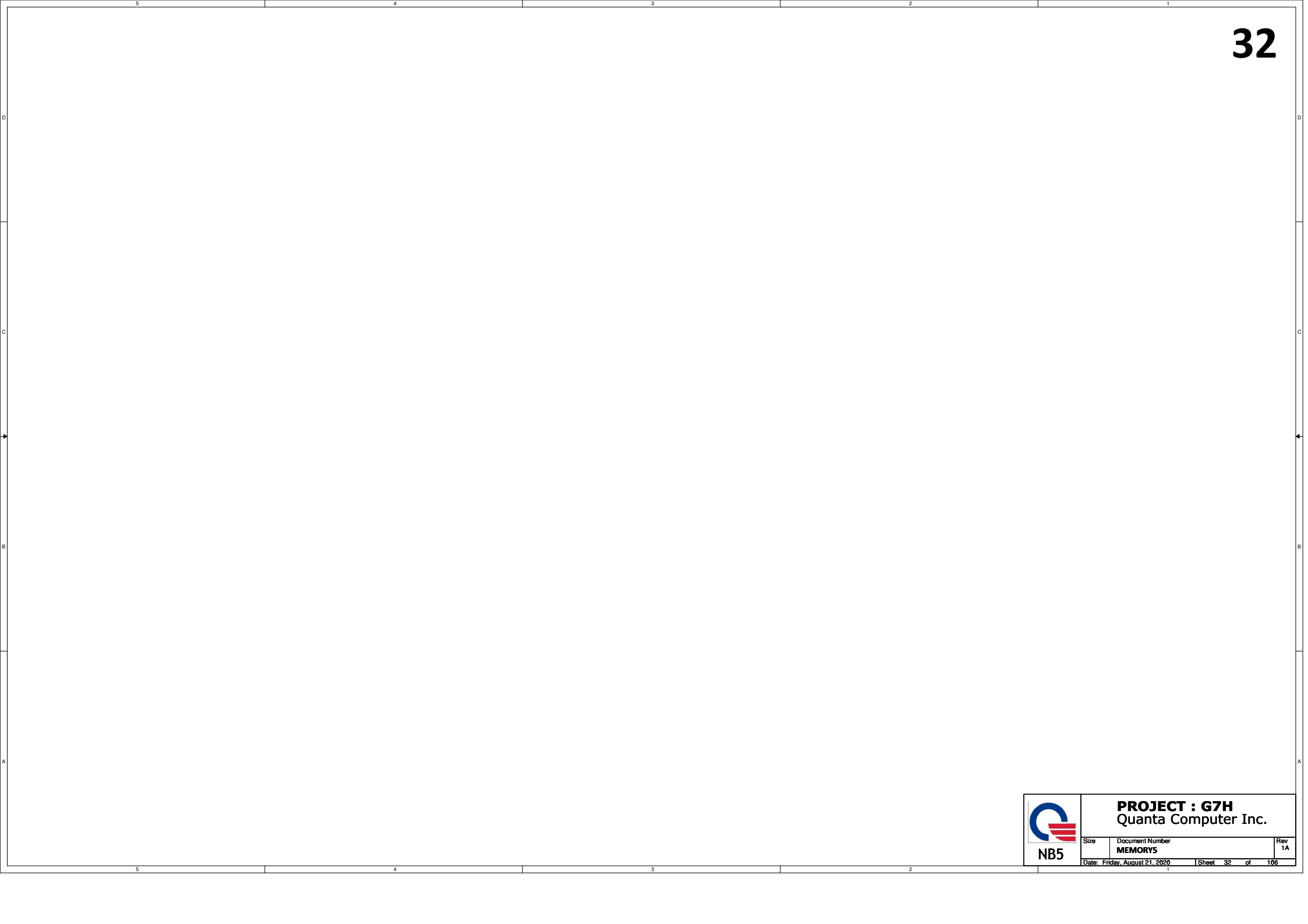
	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number PCH STRAP	Rev 1A
	Date: Friday, August 21, 2020 Sheet 27 of 106		







 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		MEMORY3	1A
Date: Friday, August 21, 2020 Sheet 30 of 106			

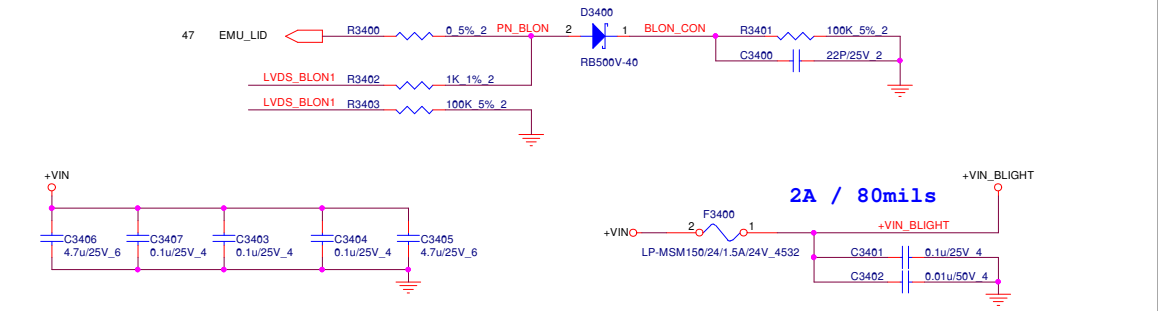
	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		MEMORY4	1A
Date: Friday, August 21, 2020 Sheet 31 of 106			



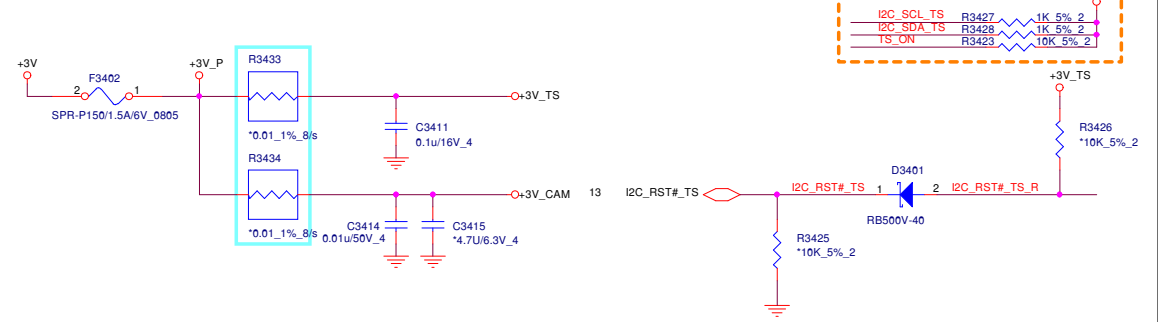
 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		MEMORY5	1A
Date: Friday, August 21, 2020 Sheet 32 of 106			

	PROJECT : G7H Quanta Computer Inc.	
	Size	Document Number
	System Power Enable	
Date: Friday, August 21, 2020		Sheet 33 of 106

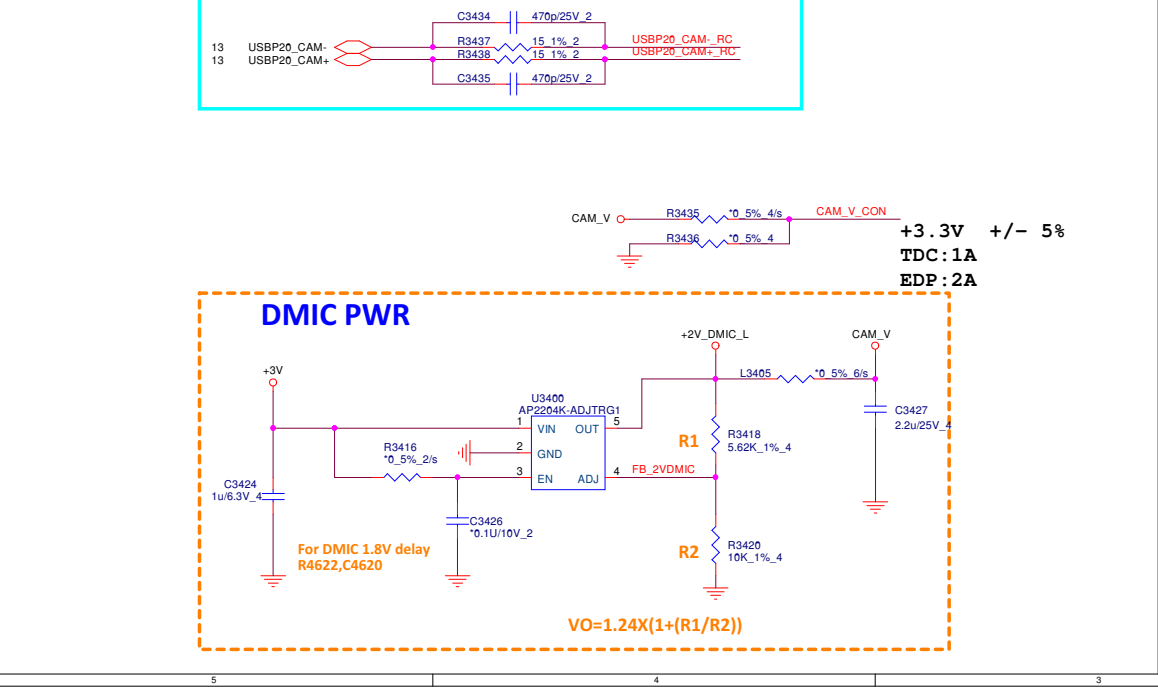
LID Switch



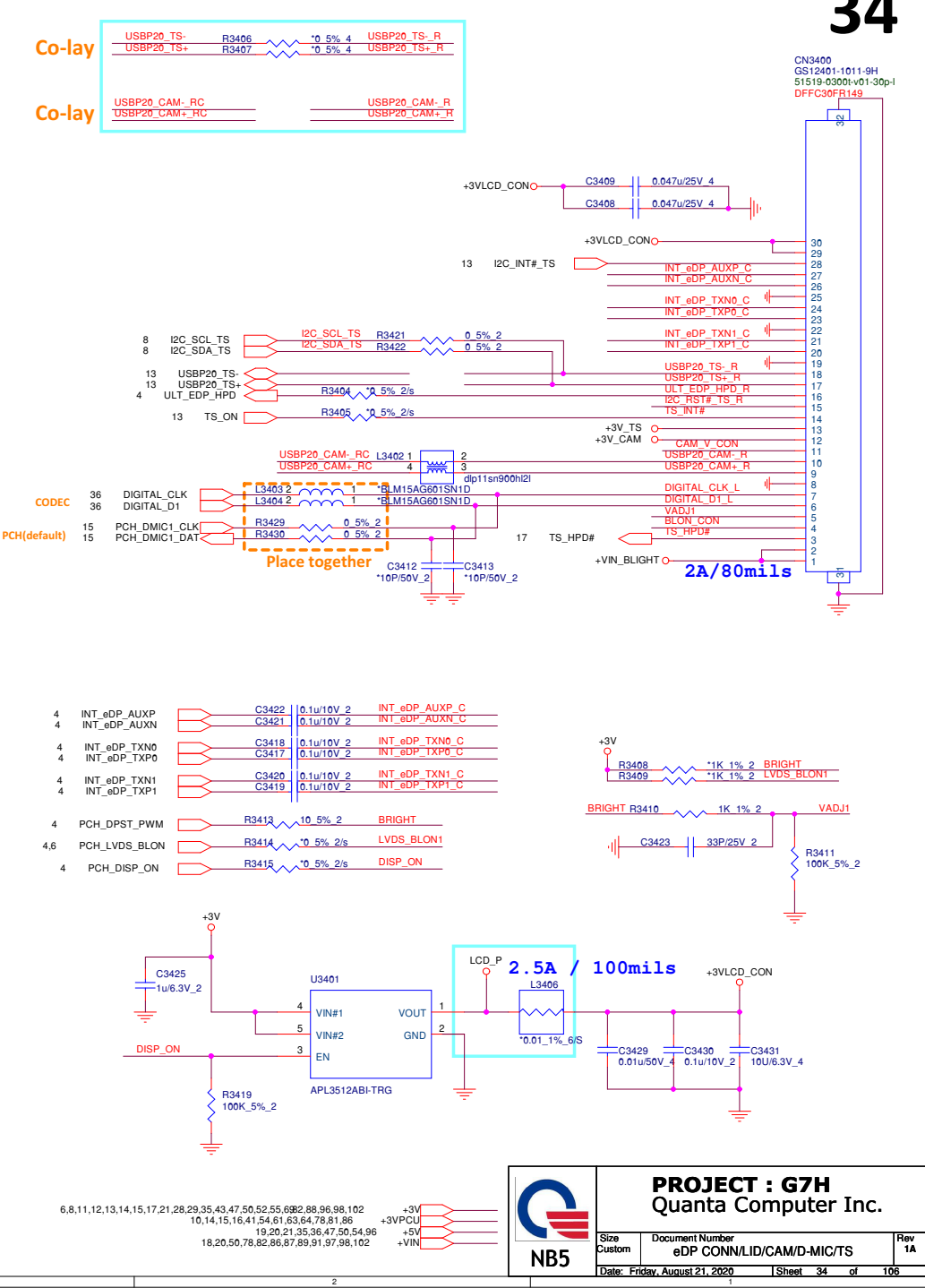
Touch screen

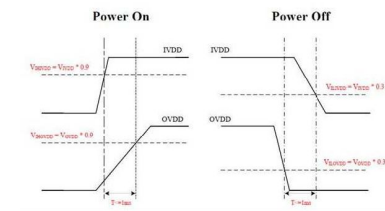
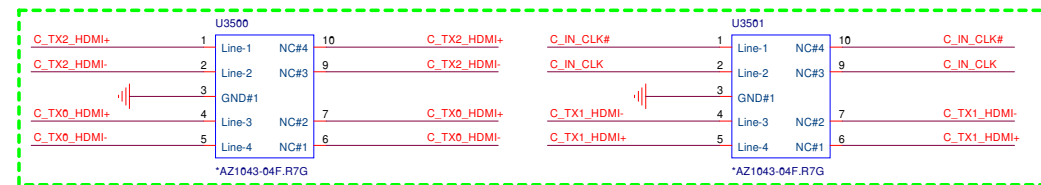
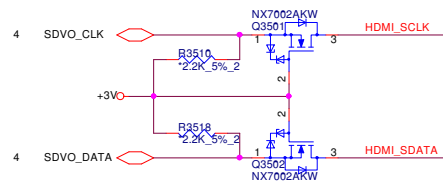
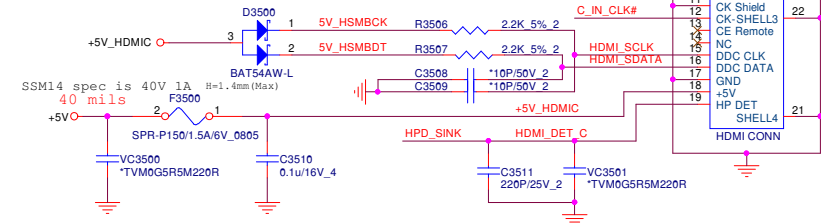


CAM



eDP Conn.





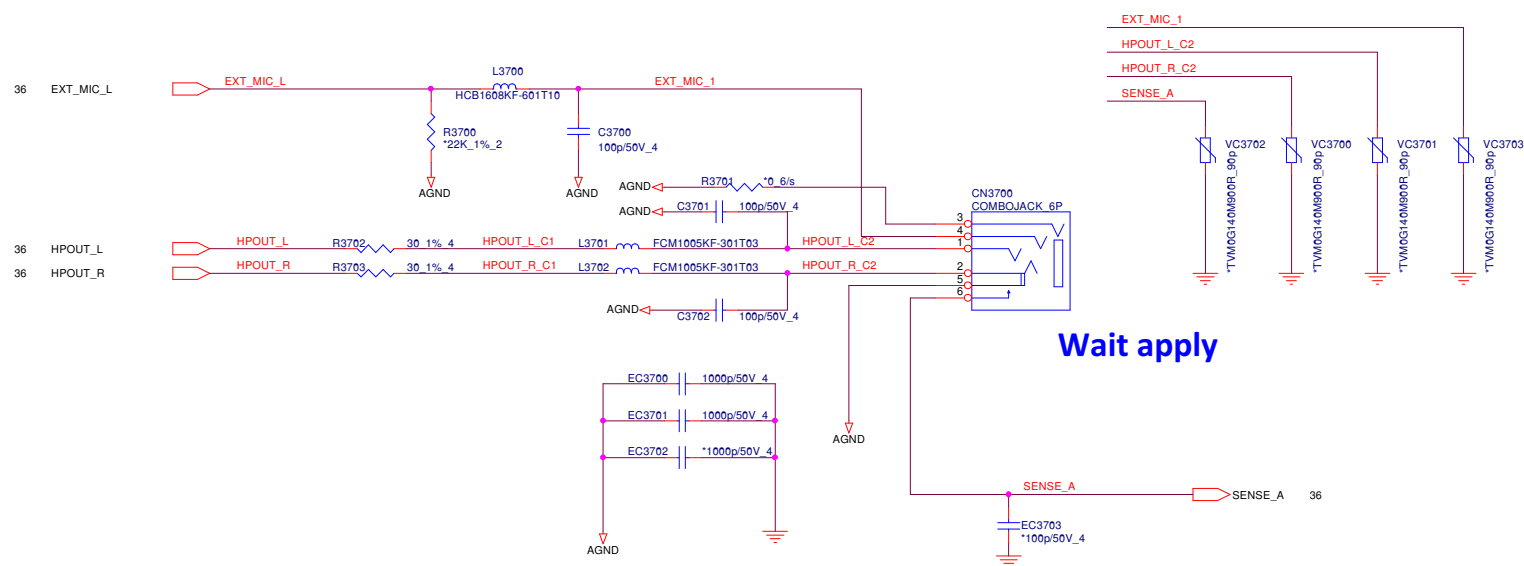
Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1


36

Size Custom	Document Number Codec ALC3314-CG	Rev 1A
Date: Friday, August 21, 2020	Sheet	36 of 106

Audio Combo Jack


Audio JACK ESD






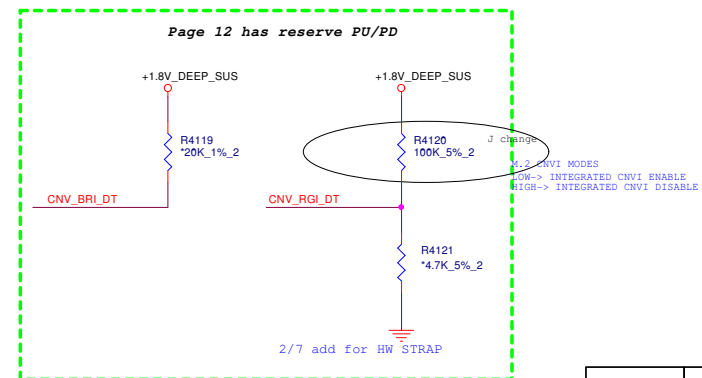
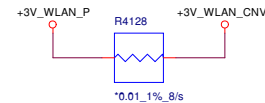
PROJECT : G7H
Quanta Computer Inc.


Size Custom	Document Number Audio	Rev 1A
Date: Friday, August 21, 2020		Sheet 38 of 106

 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number Audio	Rev 1A
	Date: Friday, August 21, 2020 Sheet 39 of 106		



	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number LAN RTL8166EH/RTL8111HSH	Rev 1A
	Date: Friday, August 21, 2020 Sheet 40 of 106		

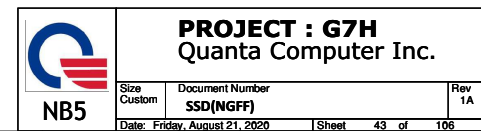





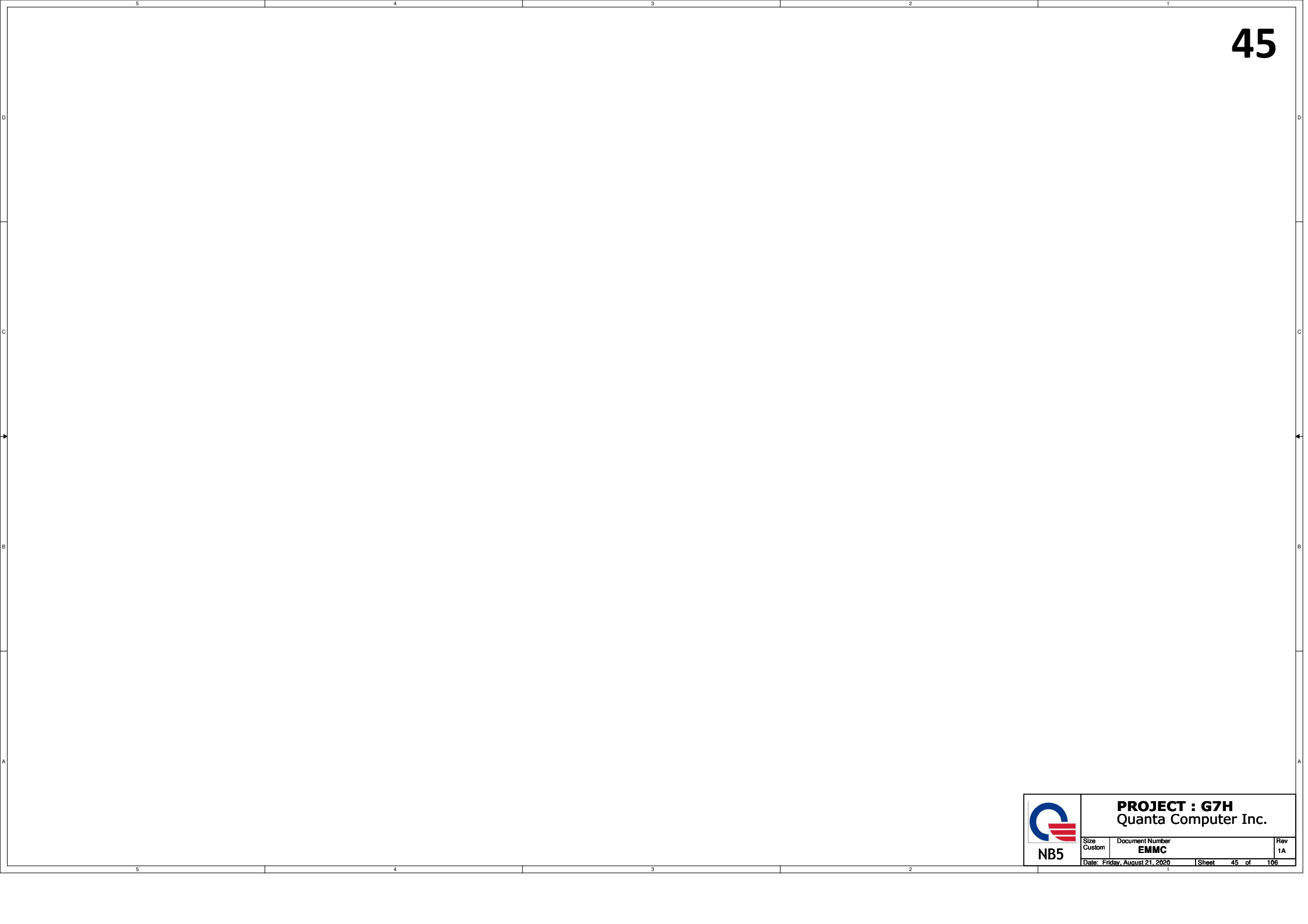
PROJECT : G7H
Quanta Computer Inc.


Size Custom	Document Number WWAN(NGFF)	Rev 1A
Date: Friday, August 21, 2020		Sheet 42 of 106


43



	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number HDD	Rev 1A
	Date: Friday, August 21, 2020 Sheet 44 of 106		

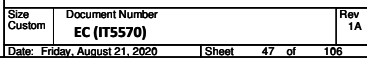



 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number EMMC	Rev 1A
	Date: Friday, August 21, 2020 Sheet 45 of 106		




PROJECT : G7H
Quanta Computer Inc.

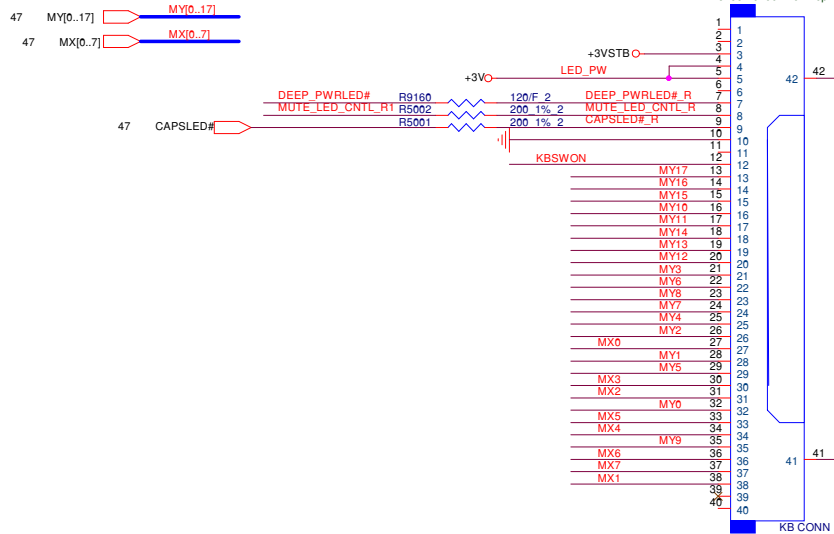
Size Custom	Document Number Camera	Rev 1A
Date: Friday, August 21, 2020		Sheet 46 of 106



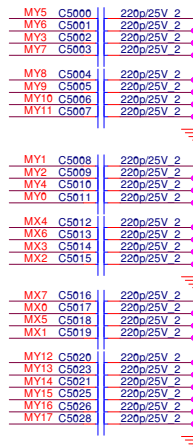
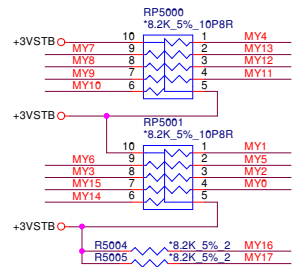
	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number EC1	Rev 1A
	Date: Friday, August 21, 2020 Sheet 48 of 106		

	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number EC2	Rev 1A
	Date: Friday, August 21, 2020 Sheet 49 of 106		

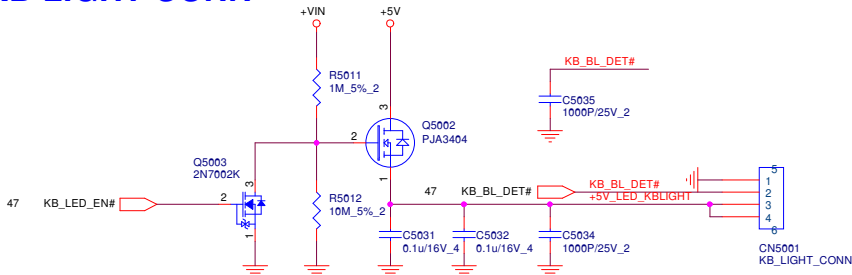
KEYBOARD Con.



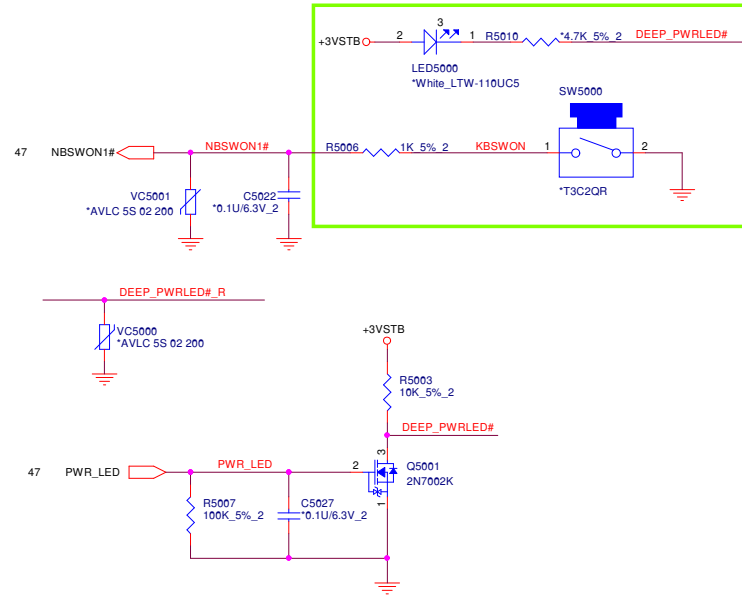
KEYBOARD PULL-UP



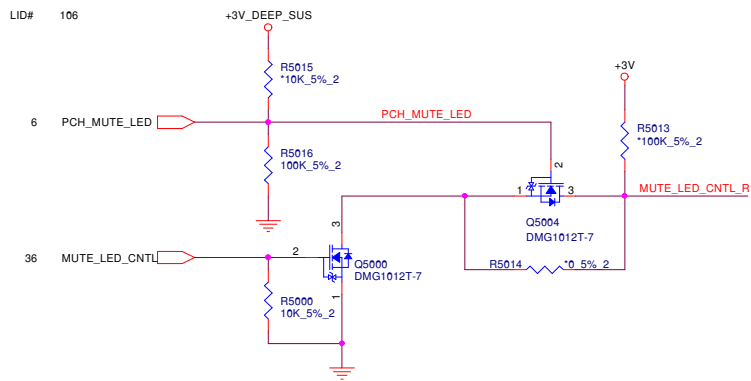
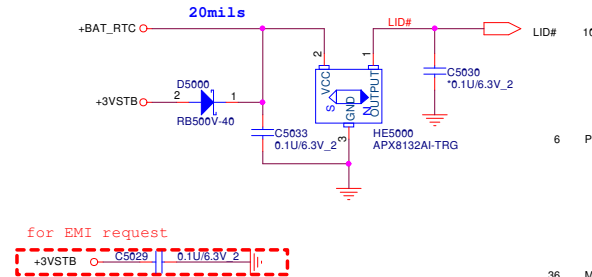
KB LIGHT CONN



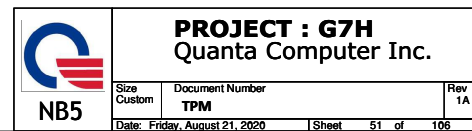
PWR Button & LED & HALL IC

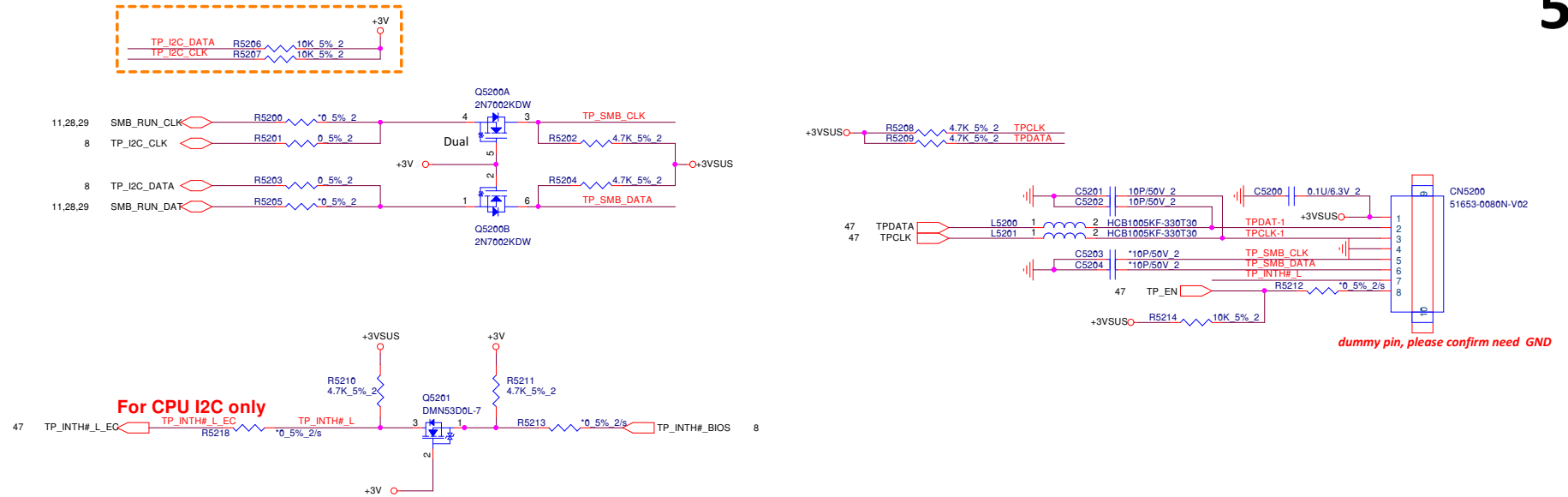


15.6" Hall sensor

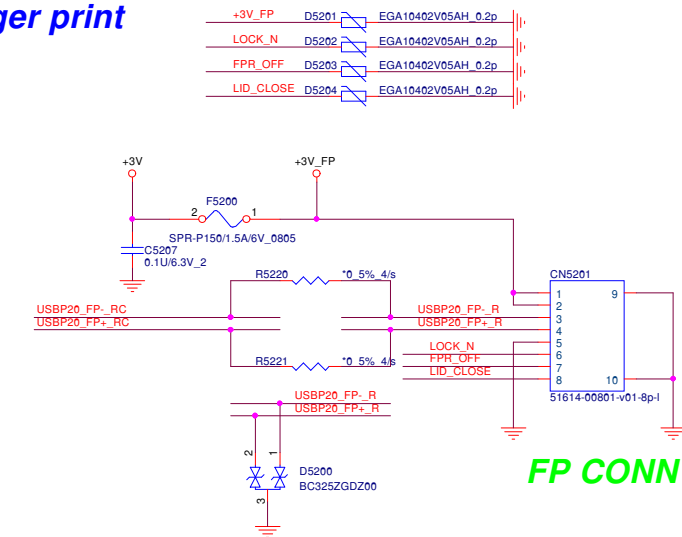


+3V_DEEP_SUS

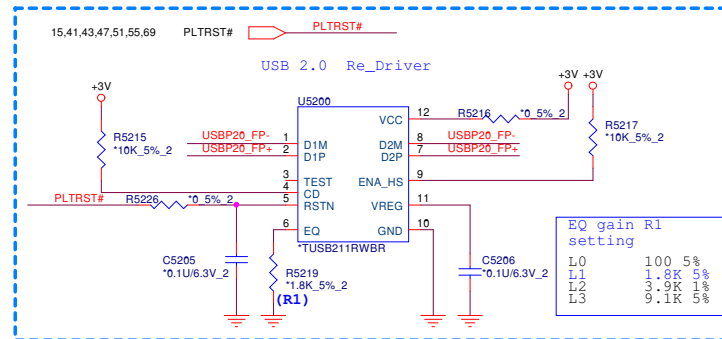




Finger print



FP CONN

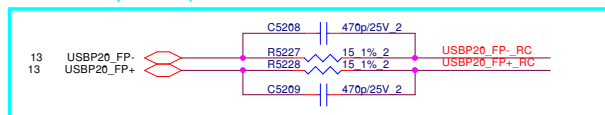



Lock_N for lock ROM data, pull high is no lock and **PCH** pull low to lock



FAE not recommend to use SLEEP mode, just only pulhigh

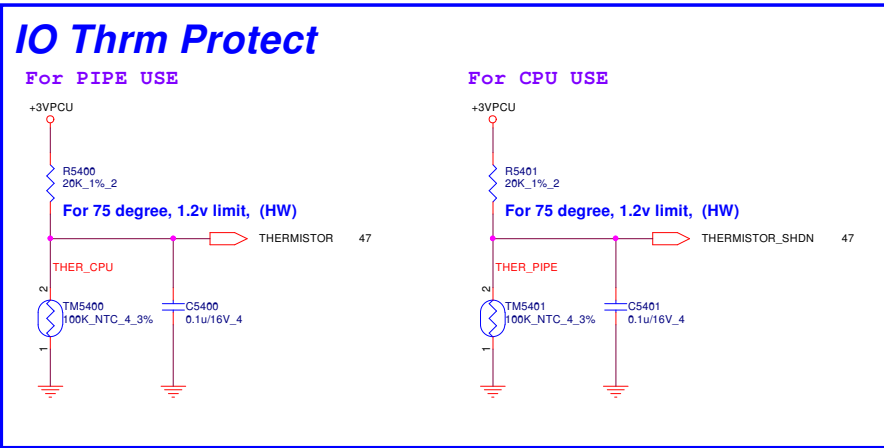
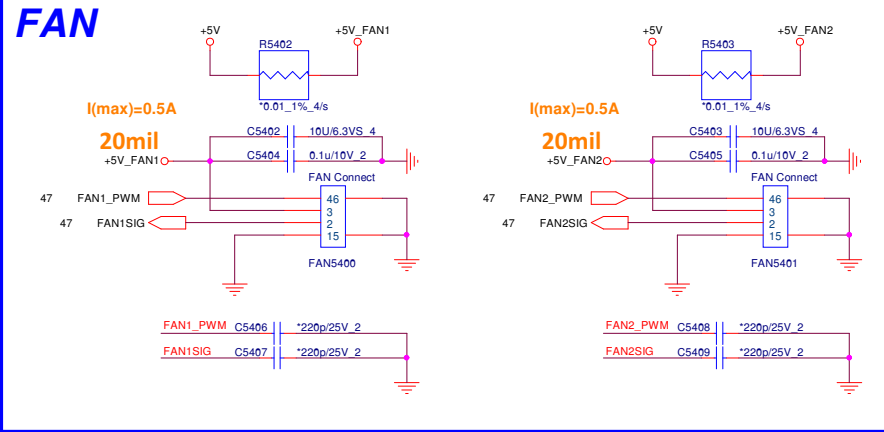
20200513 Add by Caster request





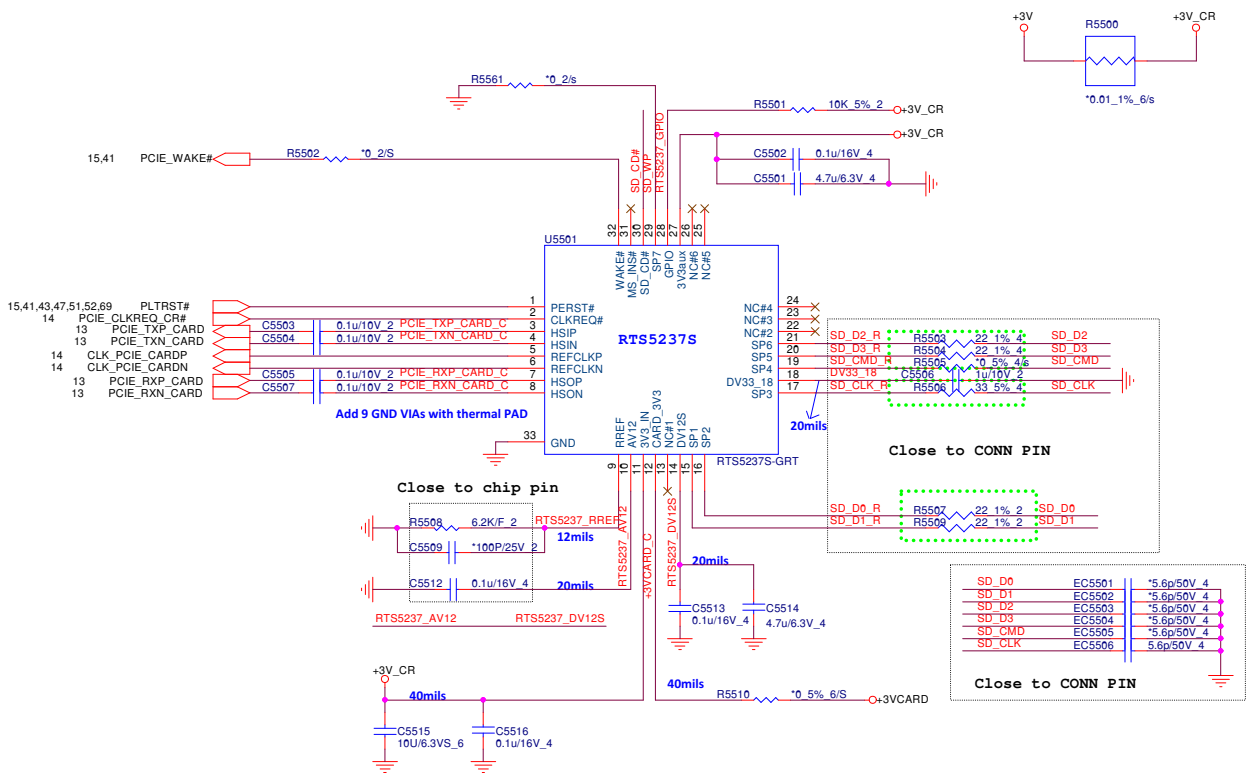
PROJECT : G7H
Quanta Computer Inc.

Size Custom	Document Number G-Sensor	Rev 1A
Date: Friday, August 21, 2020		
Sheet 53 of 106		

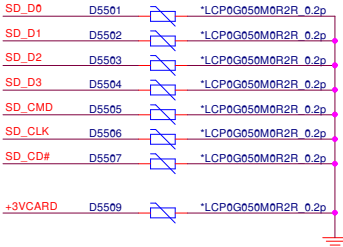
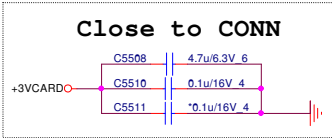
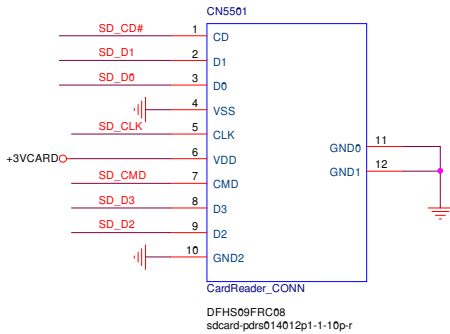


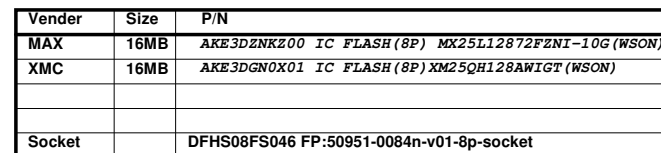
CardReader - RTS5237-GR

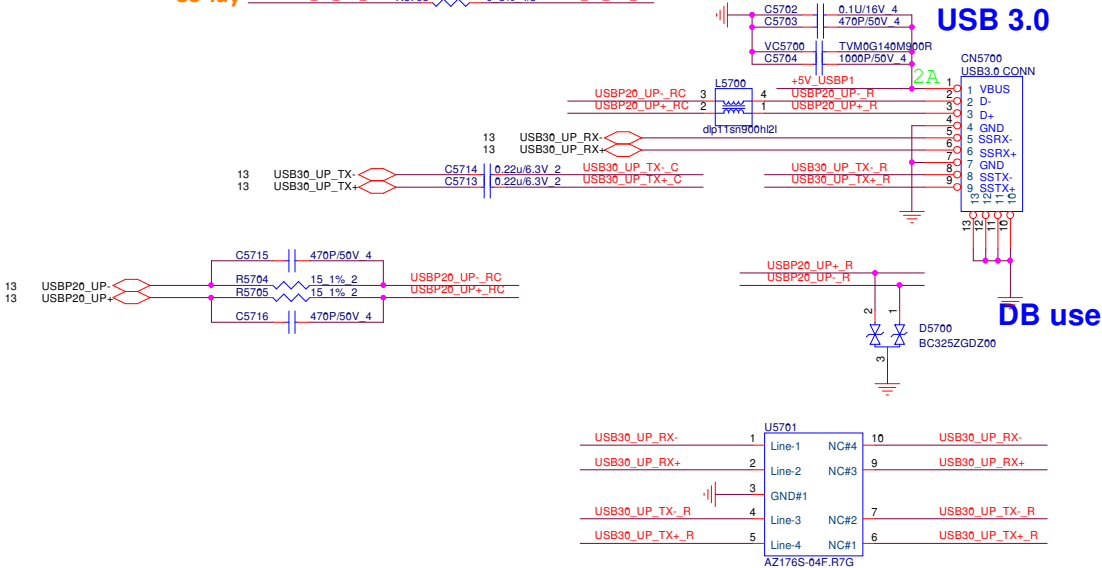
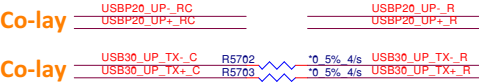
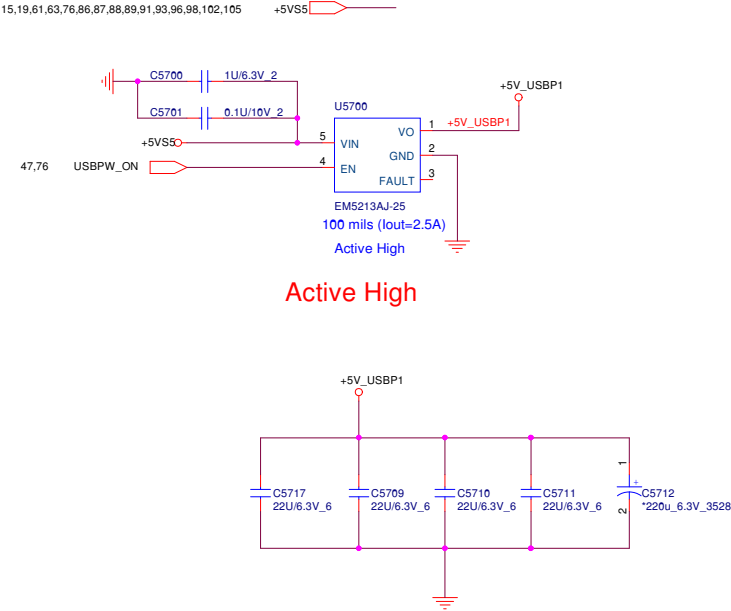
SD / MMC Share Pin





SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS




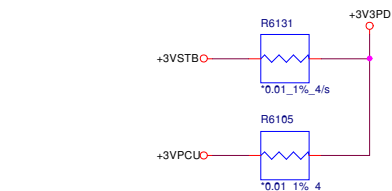




 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number Burnside Bridge Re-timer 1	Rev 1A
	Date: Friday, August 21, 2020 Sheet 58 of 106		

 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		TBT2	1A
Date: Friday, August 21, 2020 Sheet 59 of 106			

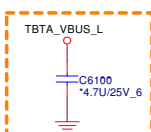
 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		TBT3	1A
Date: Friday, August 21, 2020		Sheet 60 of 106	



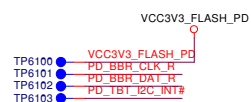
For PD debug

TP6107	PDEC_I2C_SDA
TP6108	PDEC_I2C_SCL
TP6109	SMB_PCH_DAT
TP6110	SMB_PCH_CLK
TP6111	PDEC_I2C_IRQ#
TP6112	TBT_I2C_INT#

Placed together

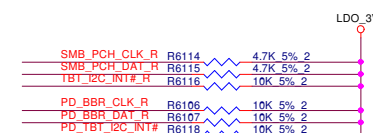
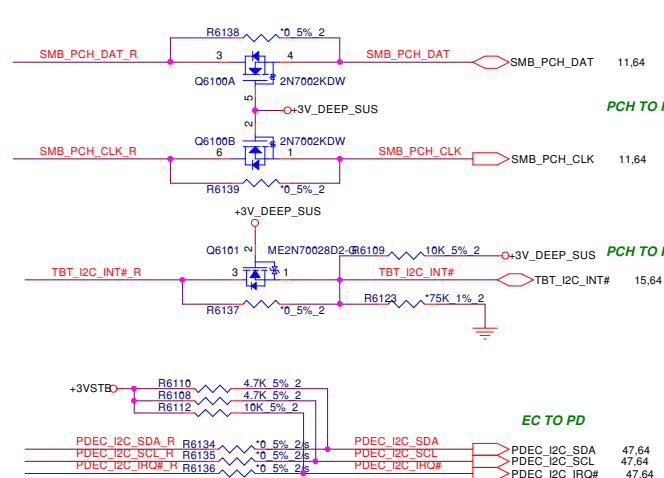
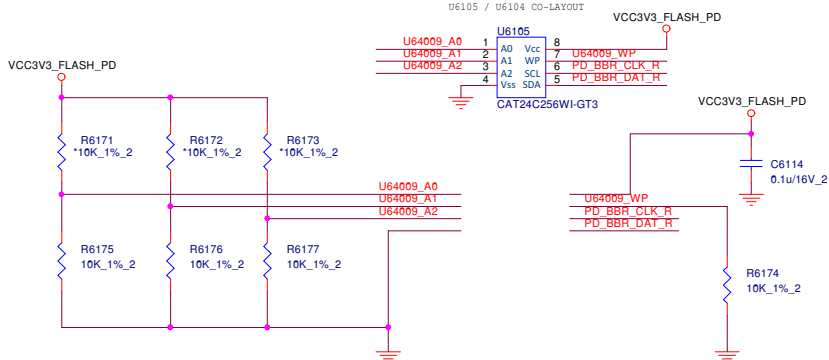


TP6100~TP6103 need place to All BOT or All TOP

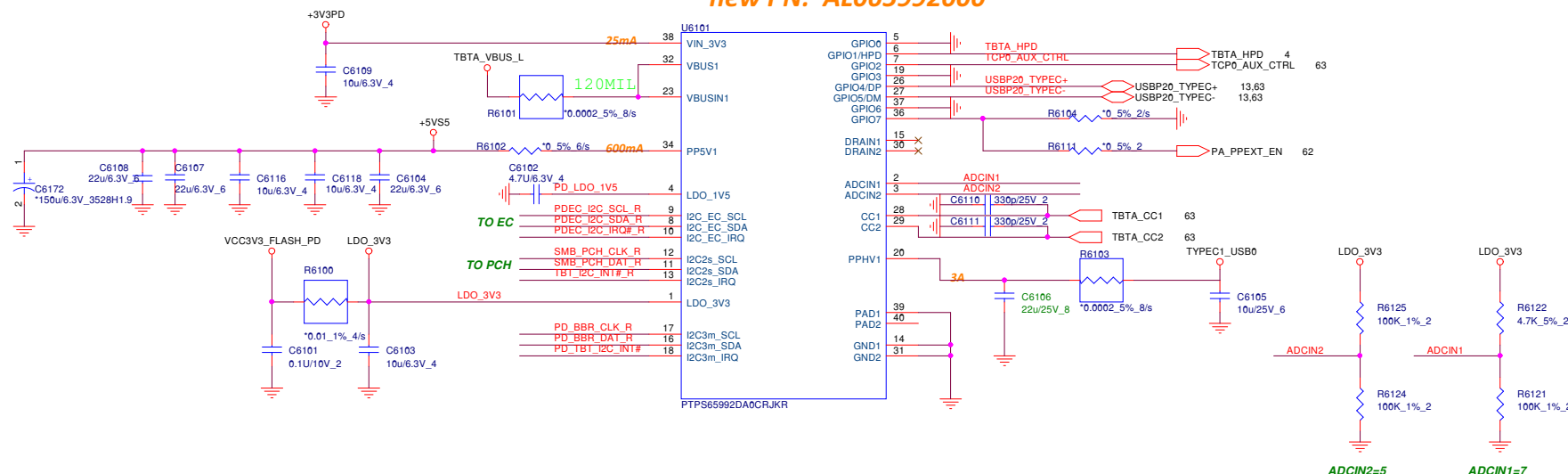


SOIC 8, 150 mils
 AKE33Z00R00 / IC EEPROM(8P) CAT24C256WI-GT3 (SOIC8)
 AKE11ZA0A00 / IC EEPROM(8P) AT24C256C-SSHL-T (SOIC)
 AKE13ZA0P00 / IC EEPROM(8P) BR24G256FJ-3AGTE2 (SOP-8)

U6105 / U6104 CO-LAYOUT



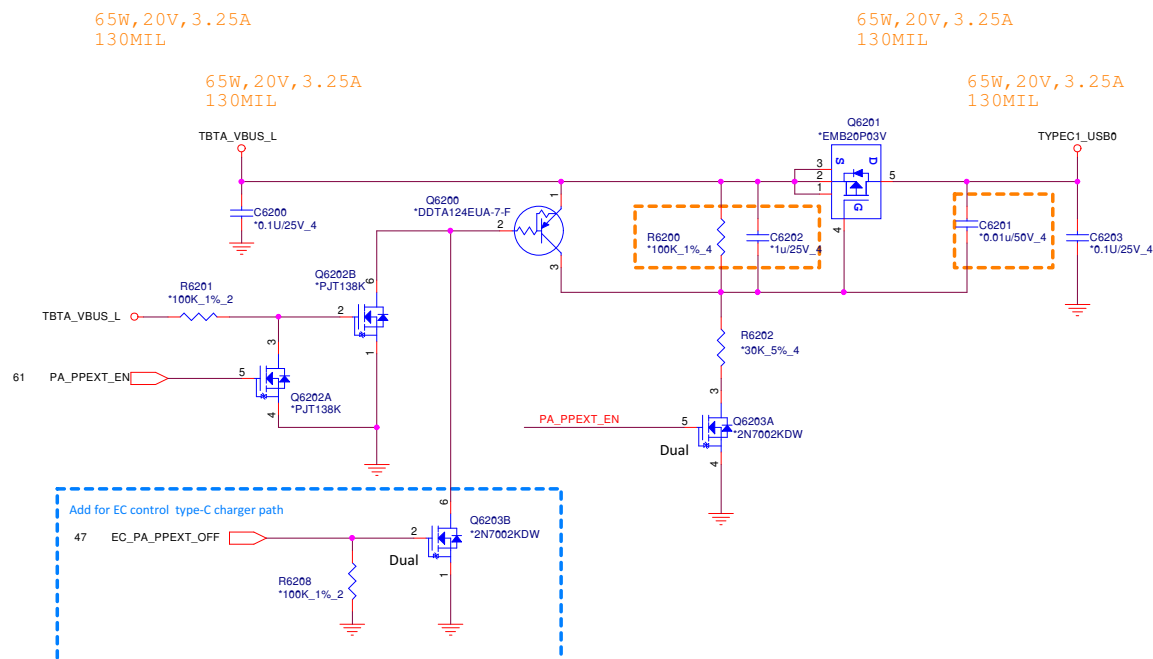
new PN: AL065992000

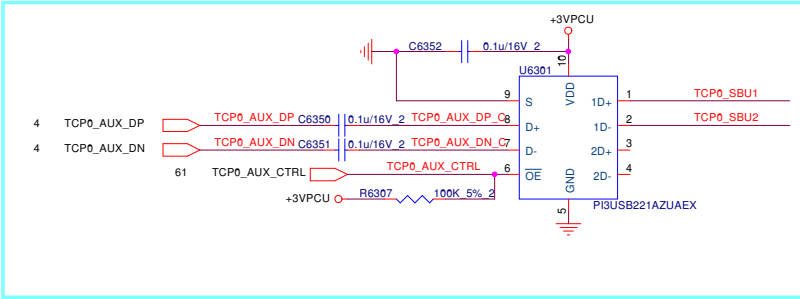
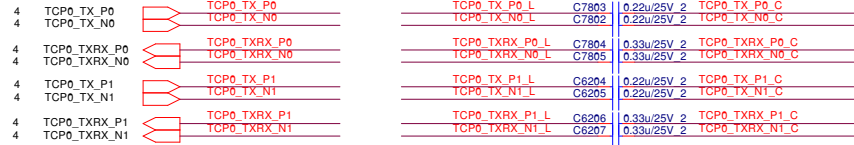
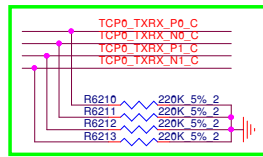
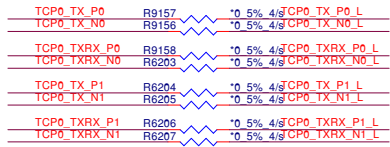


PROJECT : ABLE_TGL_13
 Quanta Computer Inc.

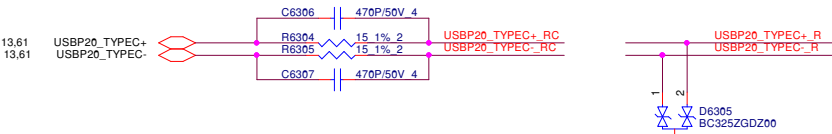
Size Custom Document Number
TPS65992D
 Date: Friday, August 21, 2020 1 Sheet 61 of 106

Rev 1A



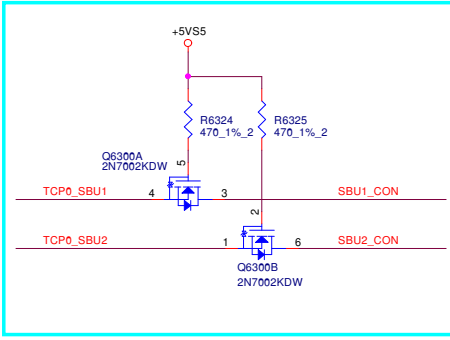
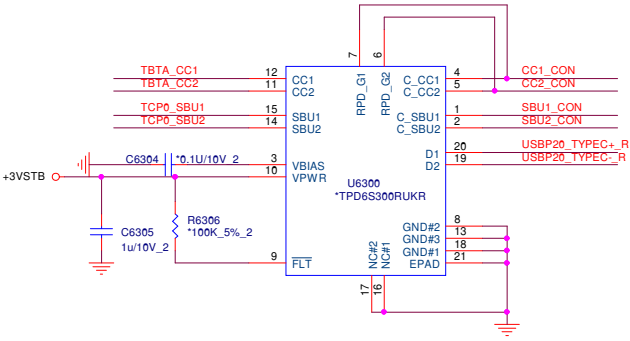


Co-lay USBP20_TYPEC+ RC R6300 0 5% 4/8 USBP20_TYPEC+ R



CC/SBU Overvoltage protection

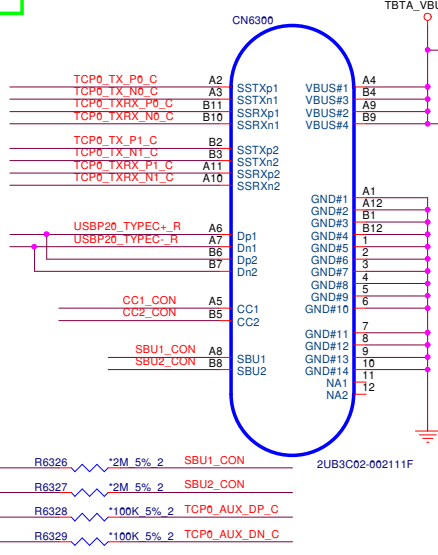
AUX MUX IC need check



0207 Add

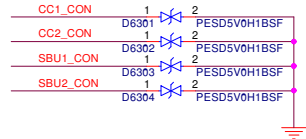
USB Type-C

65W, 20V, 3.25A
130MIL

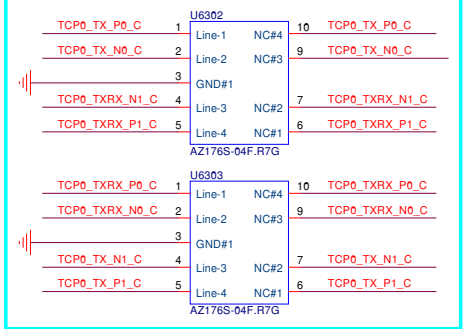


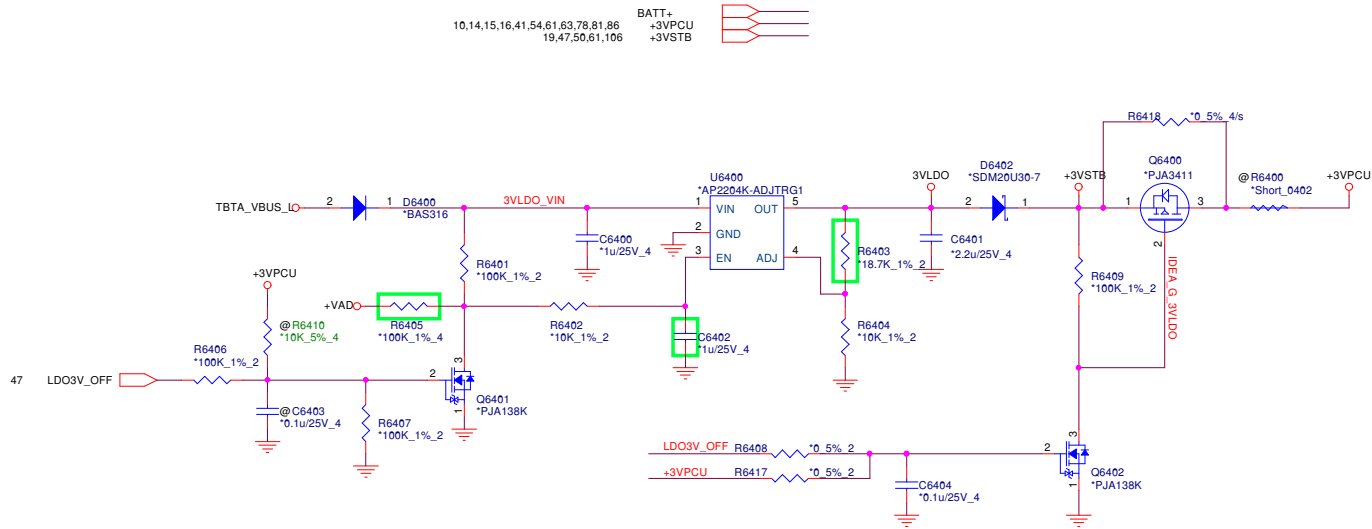
01/15 Change to DFHS24FR423 & SWAP

WAIT ESD FP

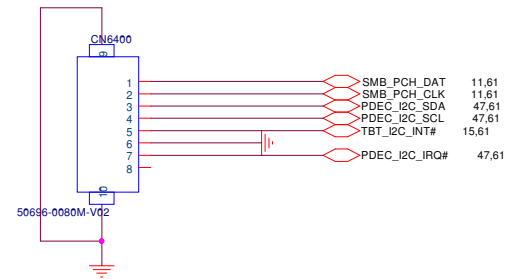


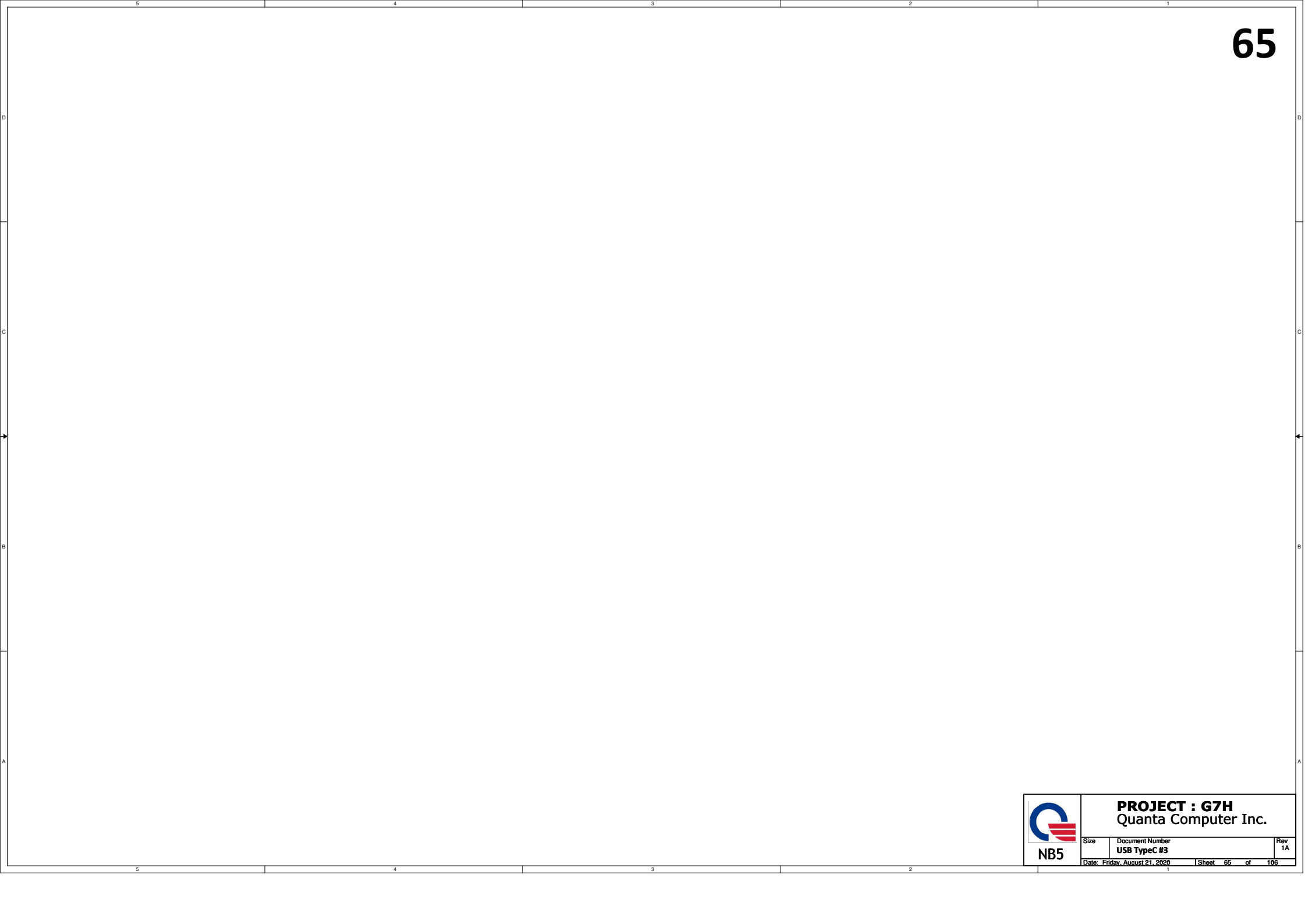
TYPE C USB3.0 ESD






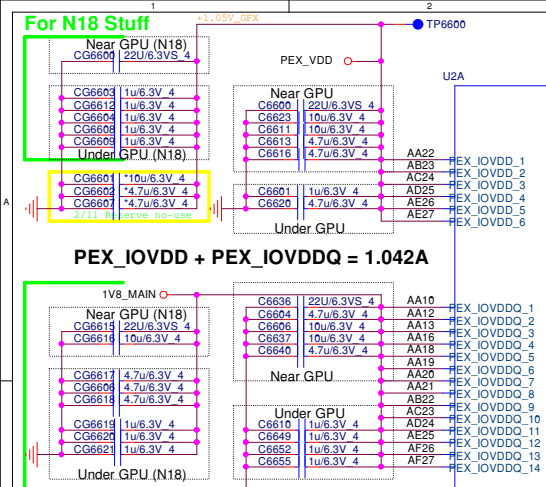
TBT/PD debug conn.





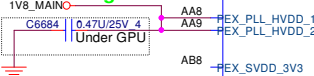
 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		USB TypeC #3	1A
Date: Friday, August 21, 2020		Sheet	65 of 106

For N18 Stuff

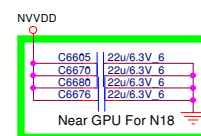
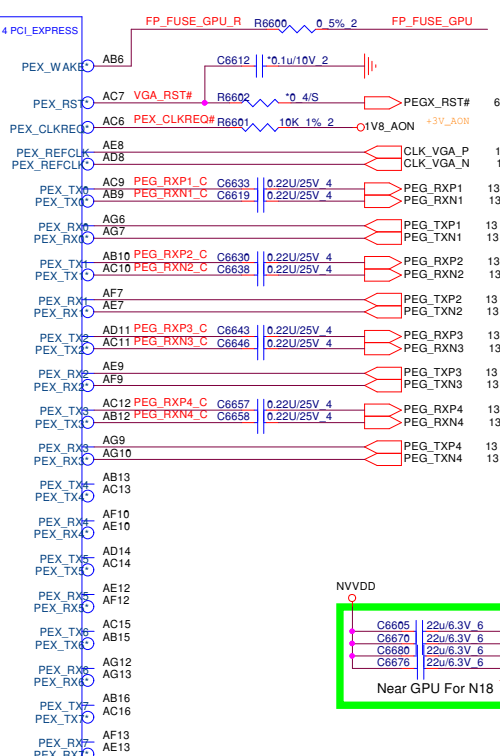


PEX_PLL_HVDD +
PEX_SVDD 3V3 = 143mA

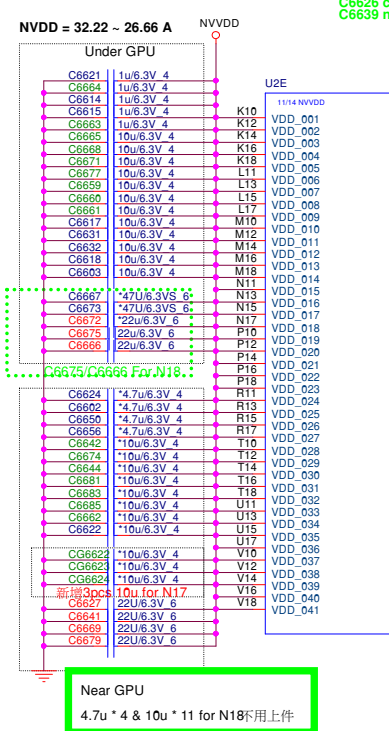
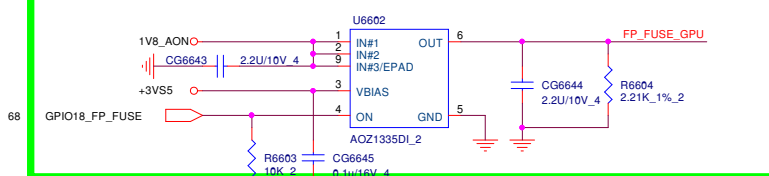
For N18 change to 0.47u



For N18 Stuff R6600

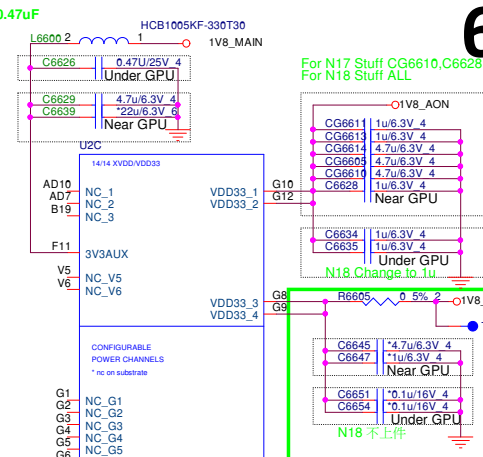


For N18 Stuff



For N18

C6626 change to 0.47uF
C6639 nun-stuff

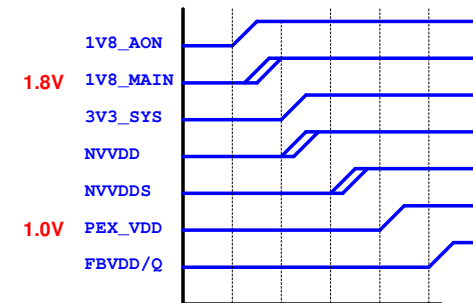


For N17 Stuff CG6610,C6628
For N18 Stuff ALL

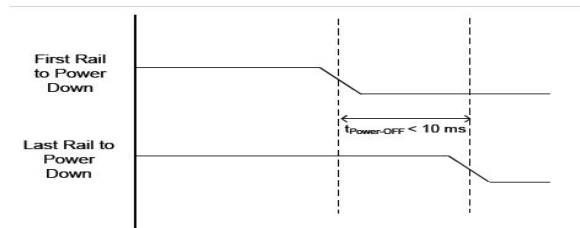
Under GPU
N18 Change to 1u

N18 不上件

Power up sequence

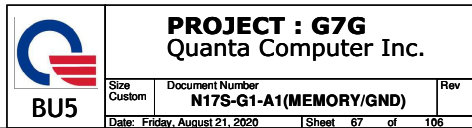


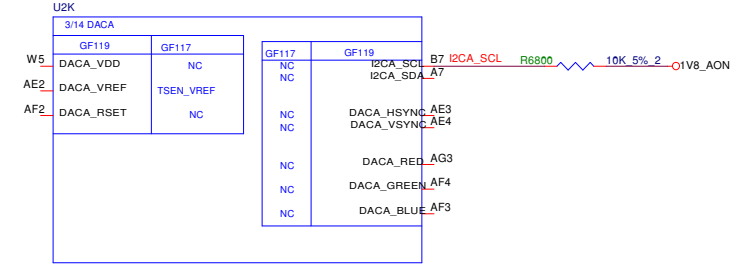
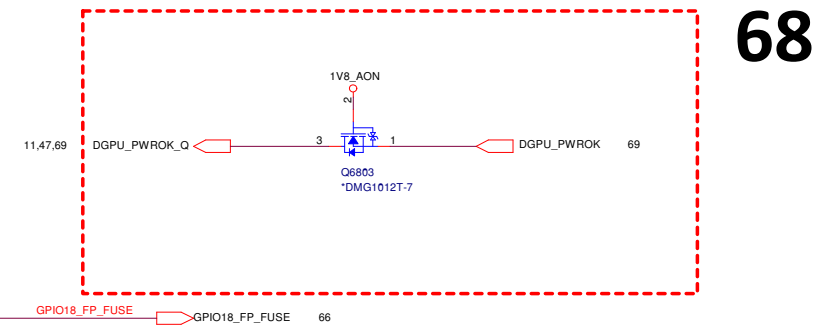
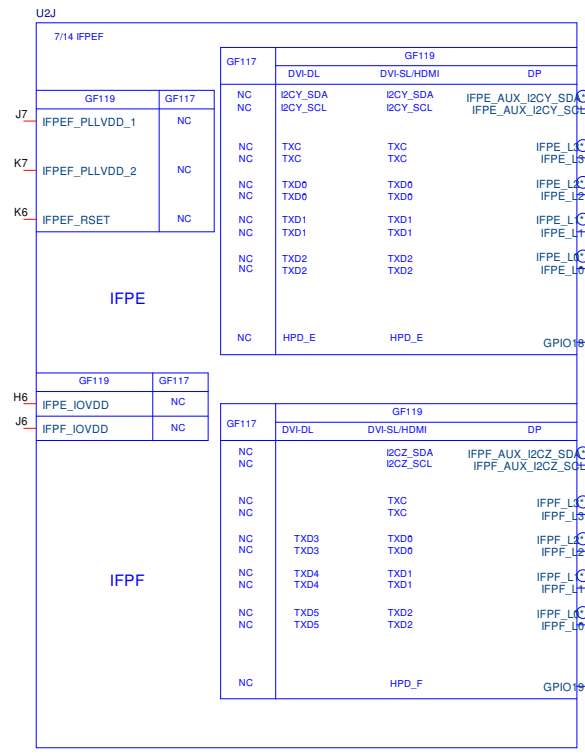
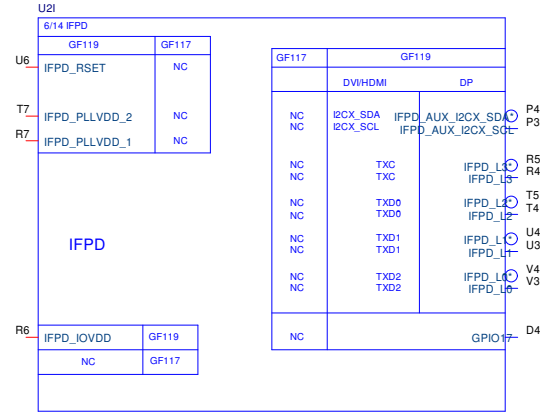
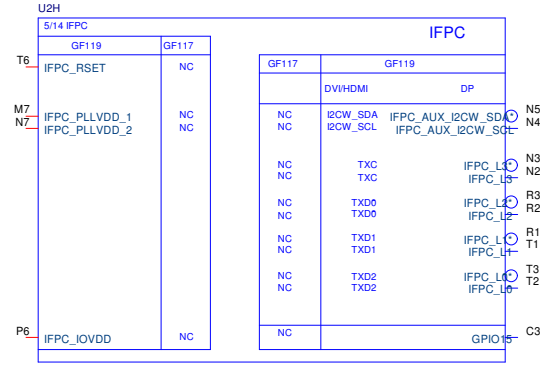
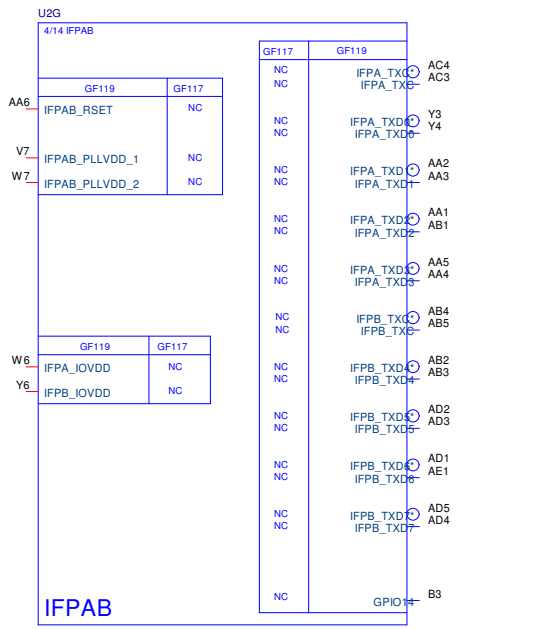
Power down sequence



PROJECT : G7G
Quanta Computer Inc.

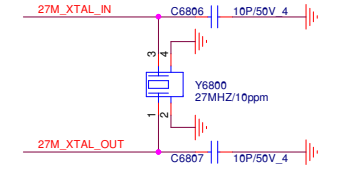
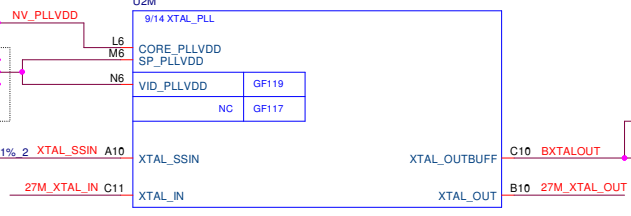
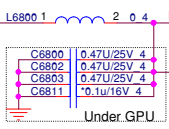
Size Custom	Document Number N17S-G1-A1(PCIE I/F)/NVDD	Re
Date: Friday, August 21, 2020	Sheet 66 of 106	



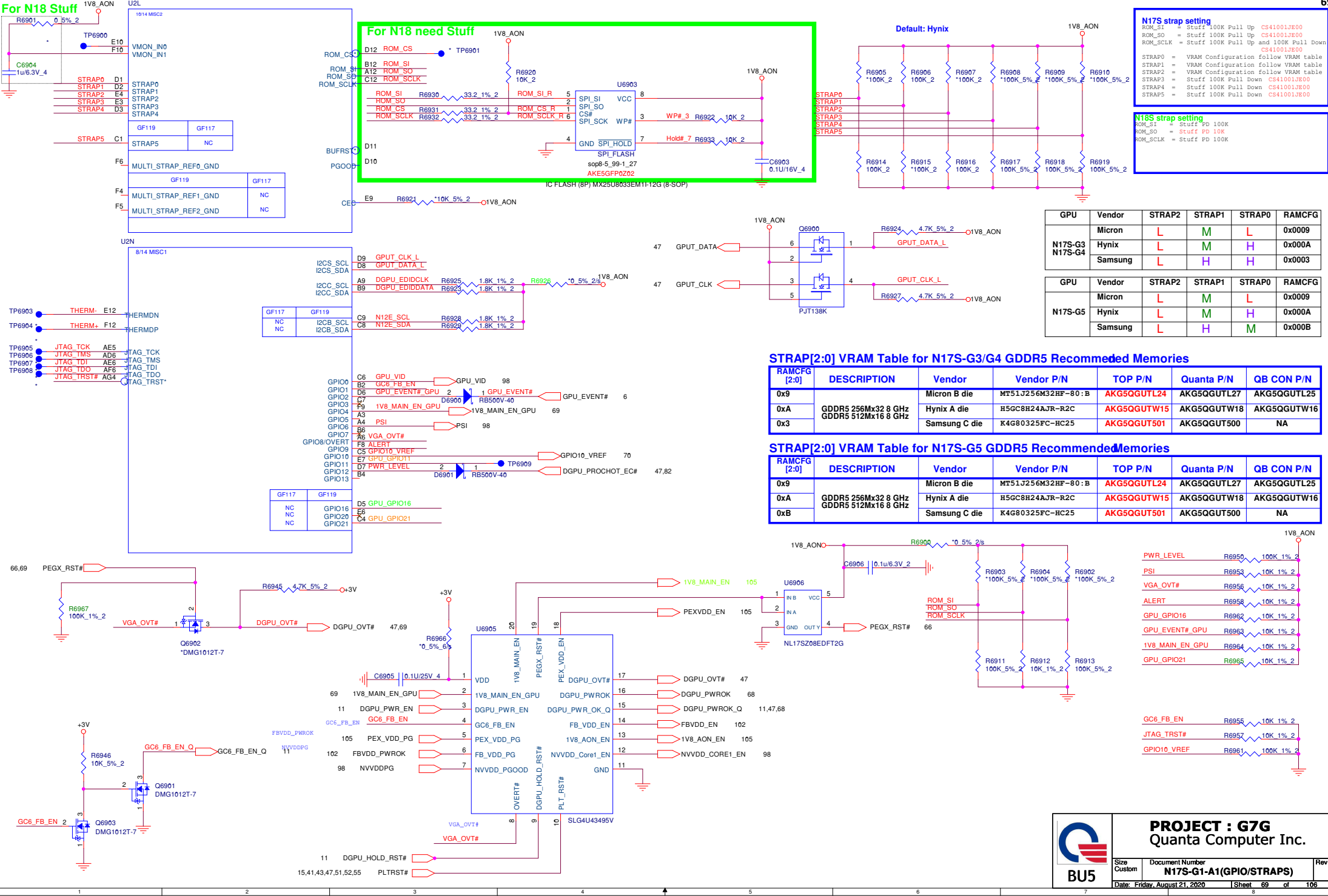


For N18 need Change
C6800,C6802,C6803 change to 0.47uF

PLLVD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA



PROJECT : G7G
Quanta Computer Inc.




GPU	Vendor	STRAP2	STRAP1	STRAP0	RAMCFG
N17S-G3 N17S-G4	Micron	L	M	L	0x0009
	Hynix	L	M	H	0x000A
	Samsung	L	H	H	0x0003

GPU	Vendor	STRAP2	STRAP1	STRAP0	RAMCFG
N17S-G5	Micron	L	M	L	0x0009
	Hynix	L	M	H	0x000A
	Samsung	L	H	M	0x000B

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	Quanta P/N	QB CON P/N
0x9		Micron B die	MT51J25M32HF-80 : B	AKG5QGUTL24	AKG5QGUTL27	AKG5QGUTL25
0xA	GDDR5 256Mx32 8 GHz GDDR5 512Mx16 8 GHz	Hynix A die	H5CG8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW18	AKG5QGUTW16
0x3		Samsung C die	K4G803235FC-HC25	AKG5QGUT501	AKG5QGUT500	NA

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	Quanta P/N	QB CON P/N
0x9	GDDR5 256Mx32 8 GHz GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL27	AKG5QGUTL25
0xA		Hynix A die	H5G8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW18	AKG5QGUTW16
0xB		Samsung C die	K4G80325FC-HC25	AKG5QGUT501	AKG5QGUT500	NA

 BU5	PROJECT : G7G Quanta Computer Inc.		
	Size Custom	Document Number N17S-G1-A1(GPIO/STRAPS)	Rev
Date: Friday, August 21, 2020		Sheet 69 of 106	

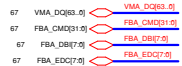
Channel A <0~31>

MF=0 Non-mirrored

CHANNEL A: 2G GDDR5

Channel A <32~63>

MF=0 Non-mirrored

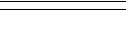
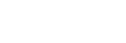
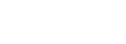
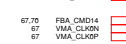
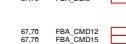
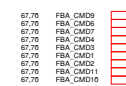


QD24~31

QD16~23

QD8~15

QD0~7

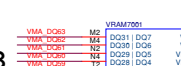
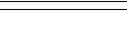
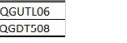
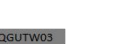
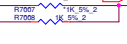


QD56~63

QD48~55

QD40~47

QD32~39

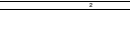
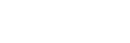
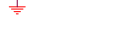
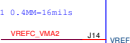
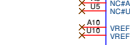
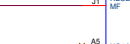
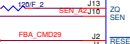
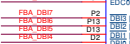
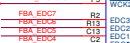
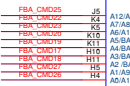


QD56~63

QD48~55

QD40~47

QD32~39

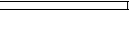
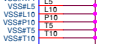
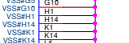
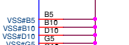
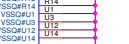
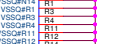
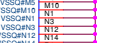
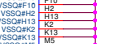
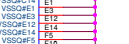
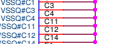
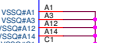
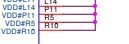
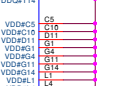


QD56~63


QD48~55


QD40~47

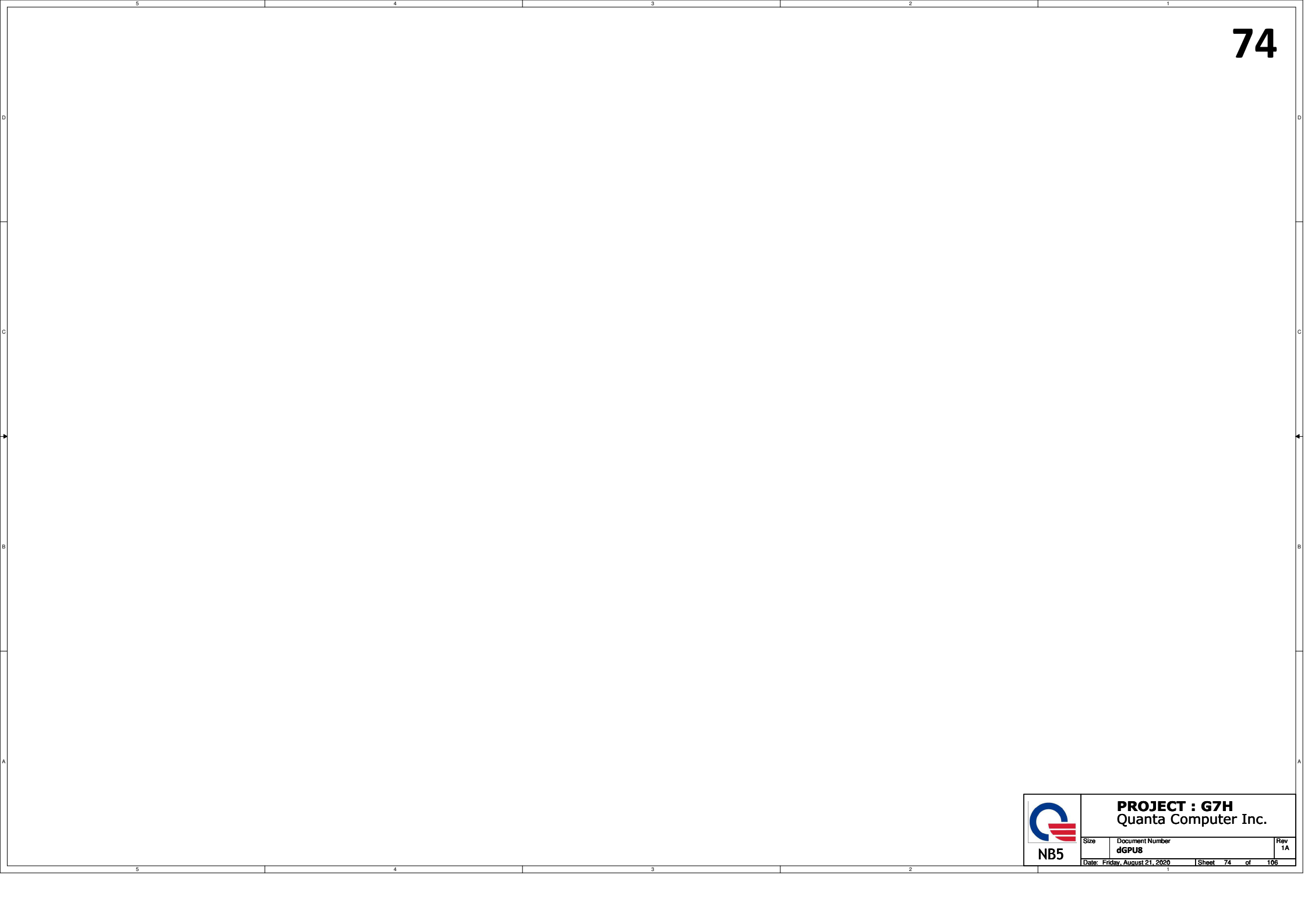
QD32~39




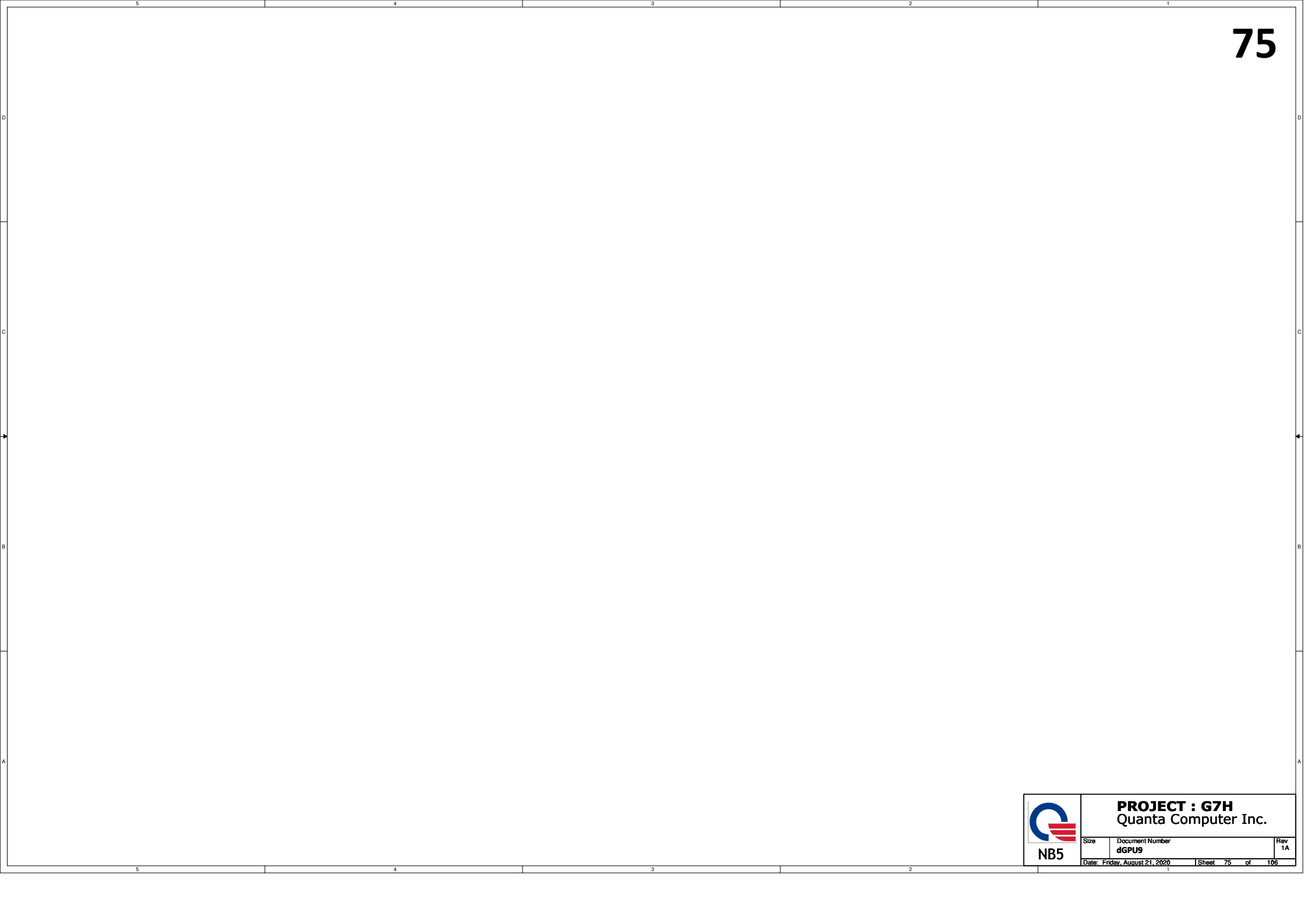
GDDR5	Hynix H5GC8H24MJR-R0C	AKG5QGUTW04	AKG5QGUTW03
256 x 32	Micron MT51J256M32HF-70:A	AKG5QGUTL07	AKG5QGUTL06
	Samsung K4G80325FD-1C2B	AKG5QDGT509	AKG5QDGT508


	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		dGPU6	1A
Date: Friday, August 21, 2020 Sheet 72 of 106			

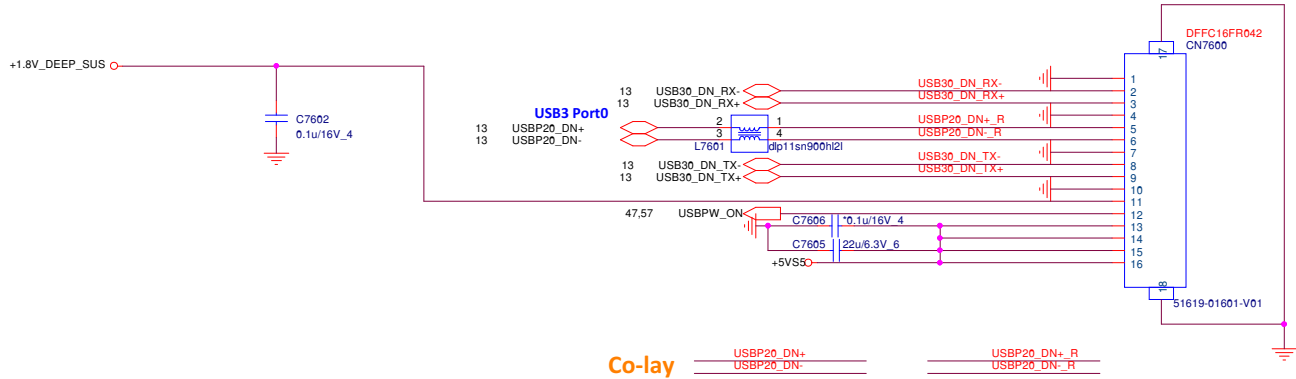
	PROJECT : G7H Quanta Computer Inc.	
	Size	Document Number
	dGPU7	
Date: Friday, August 21, 2020		Sheet 73 of 106



	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		dGPU8	1A
Date: Friday, August 21, 2020 Sheet 74 of 106			



 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		dGPU9	1A
Date: Friday, August 21, 2020 Sheet 75 of 106			



PROJECT : G7H
Quanta Computer Inc.

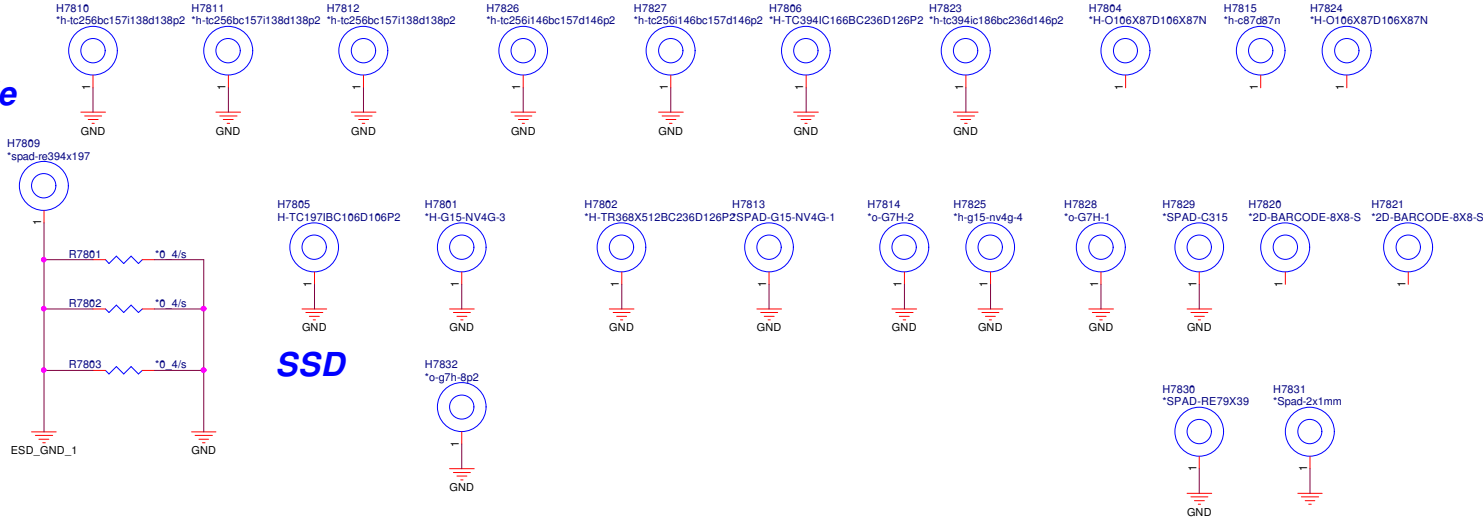
Size Custom	Document Number Daughter Board	Rev 1A
Date: Friday, August 21, 2020		

6,8,11,12,13,14,15,17,21,28,29,34,35,43,47,50,52,59,82,88,96,98,102

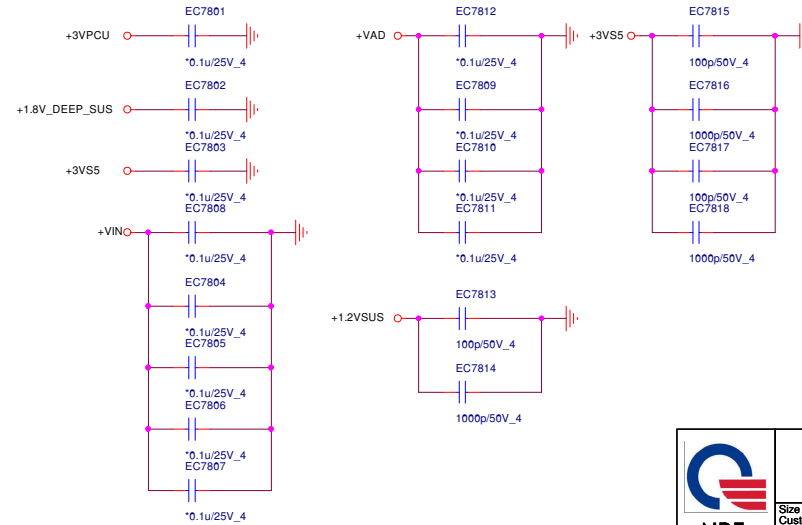
+3V




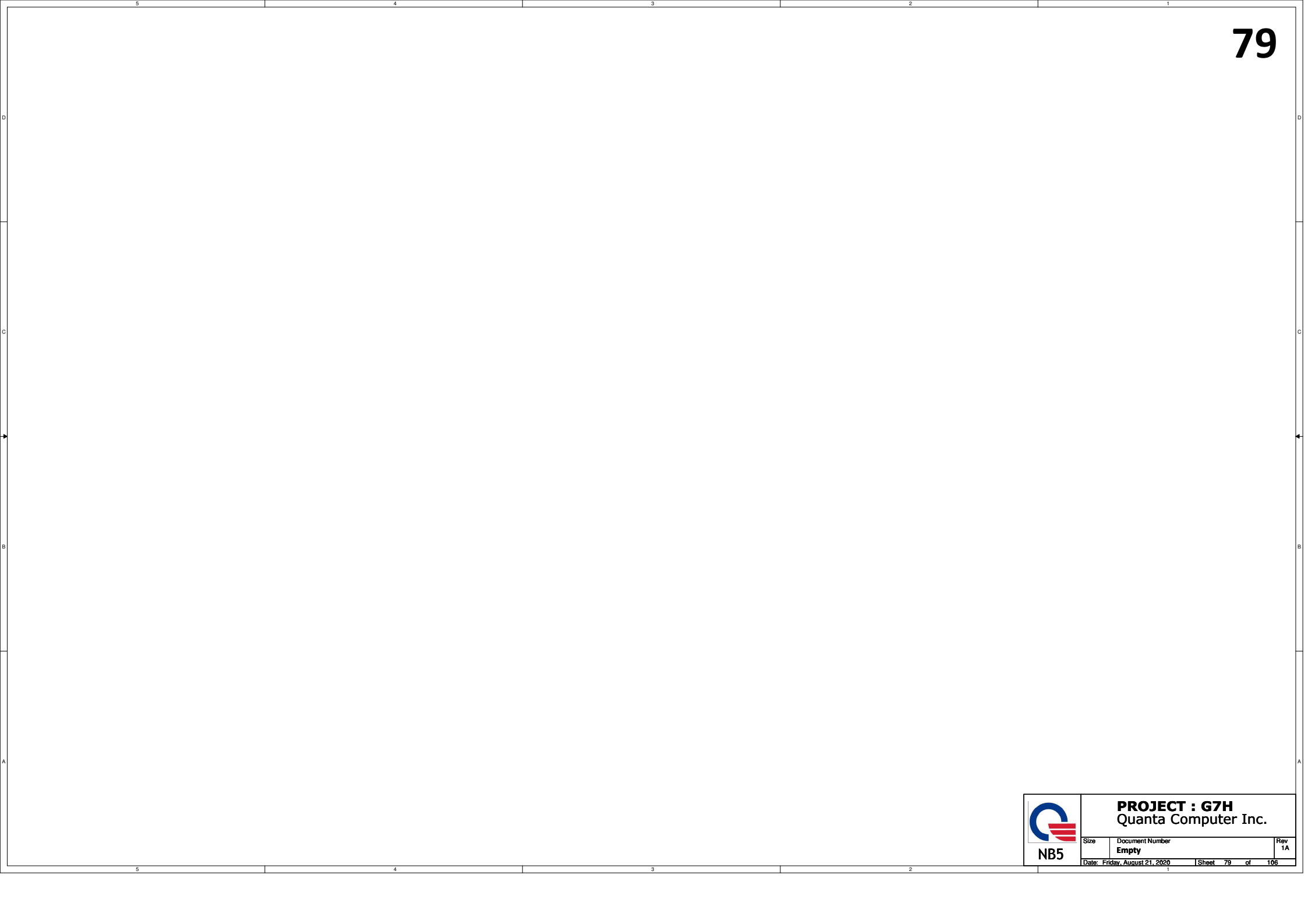
Hole




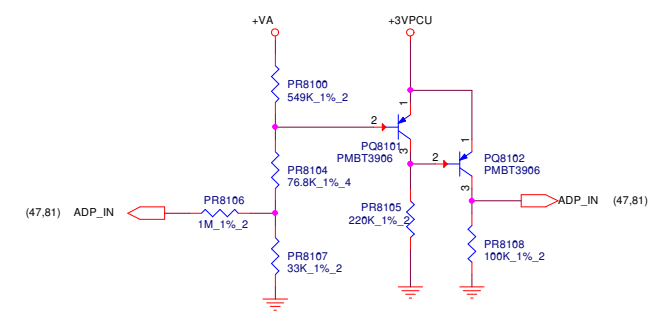
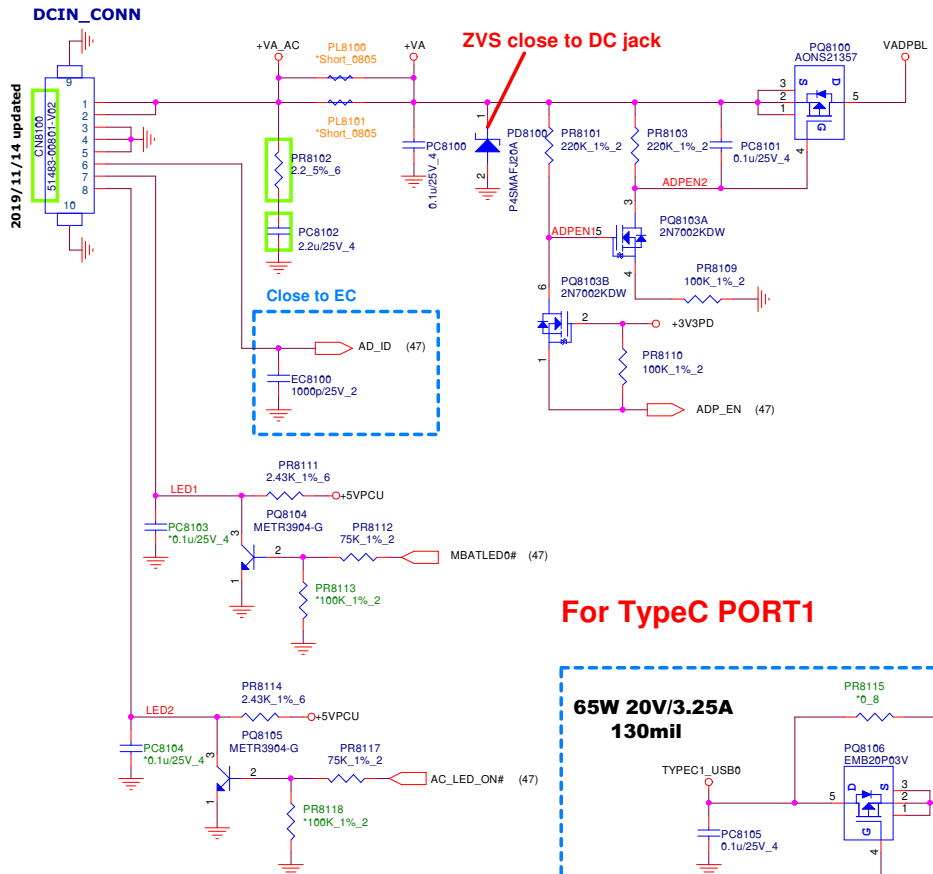
EMI Solution



 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number EMI solution/HOLE	Rev 1A
	Date: Friday, August 21, 2020 Sheet 78 of 106		

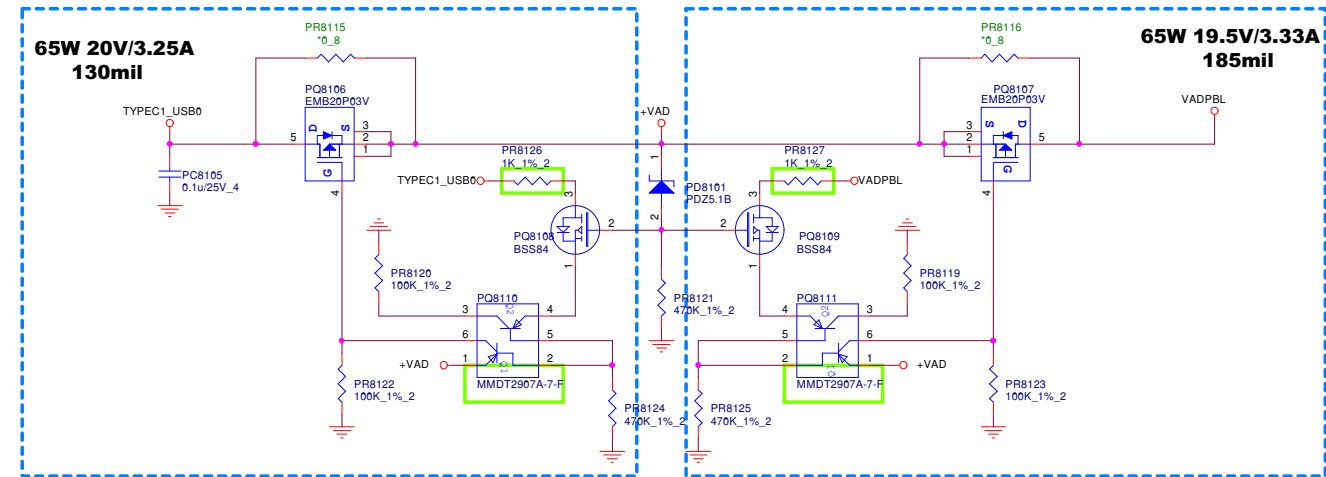


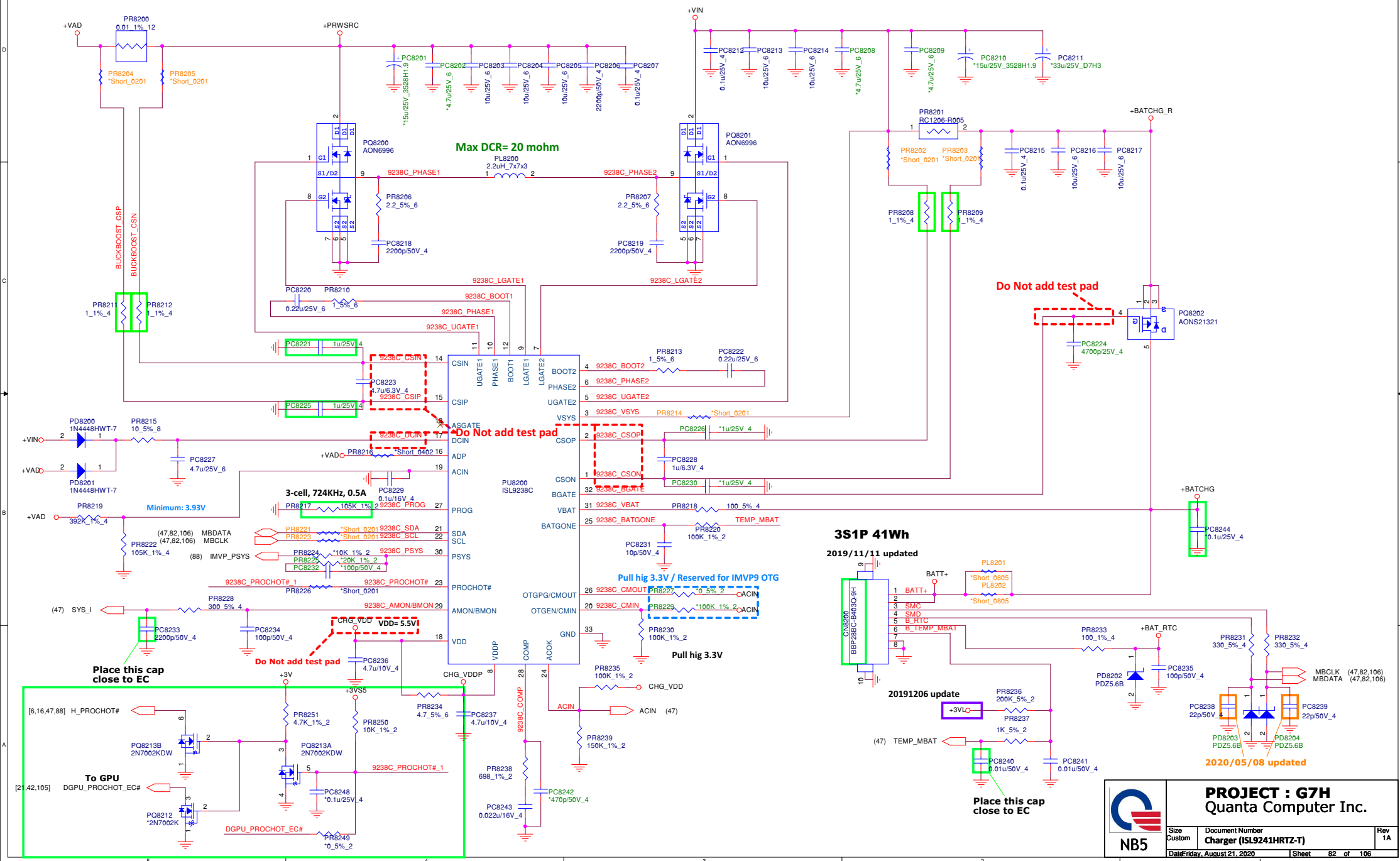
	PROJECT : G7H Quanta Computer Inc.		
	Size	Document Number	Rev
		Empty	1A
Date: Friday, August 21, 2020 Sheet 79 of 106			




For TypeC PORT1

For Barrel port








PROJECT : G7H
Quanta Computer Inc.

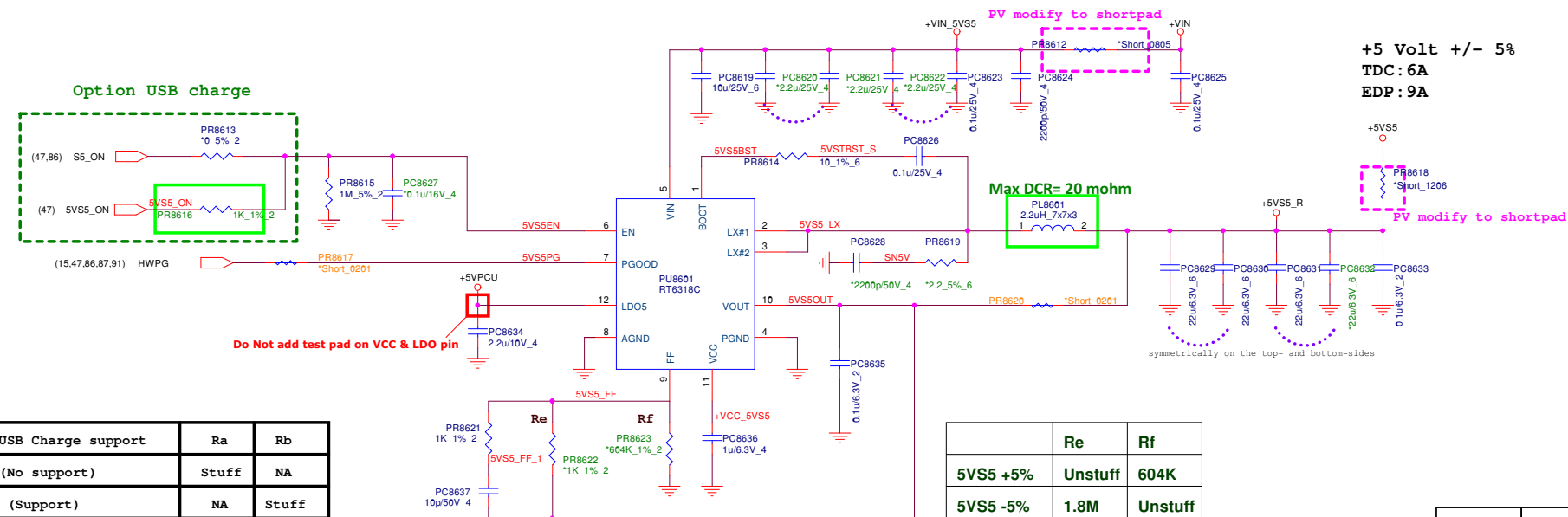
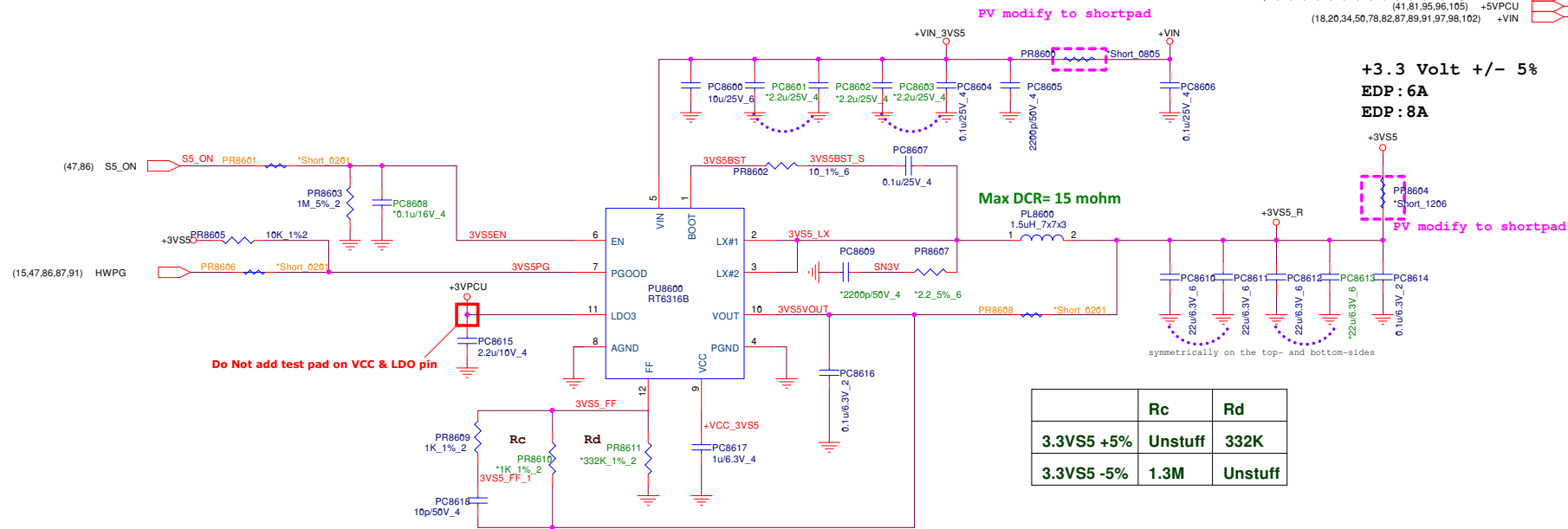
Size Custom	Document Number 98 -- reserve page(N.A)	Rev 1A
Date: Friday, August 21, 2020		Sheet 83 of 106



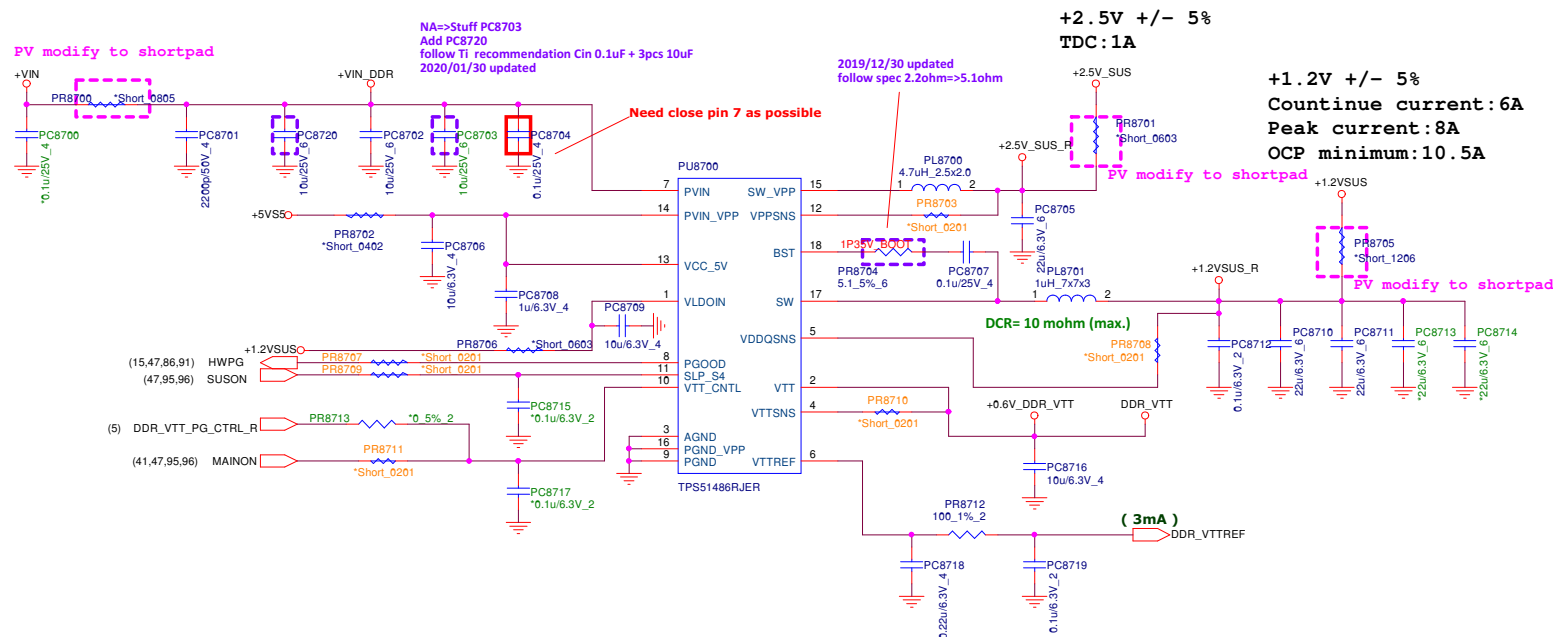
PROJECT : G7H
Quanta Computer Inc.

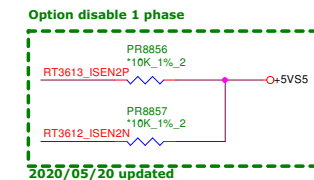
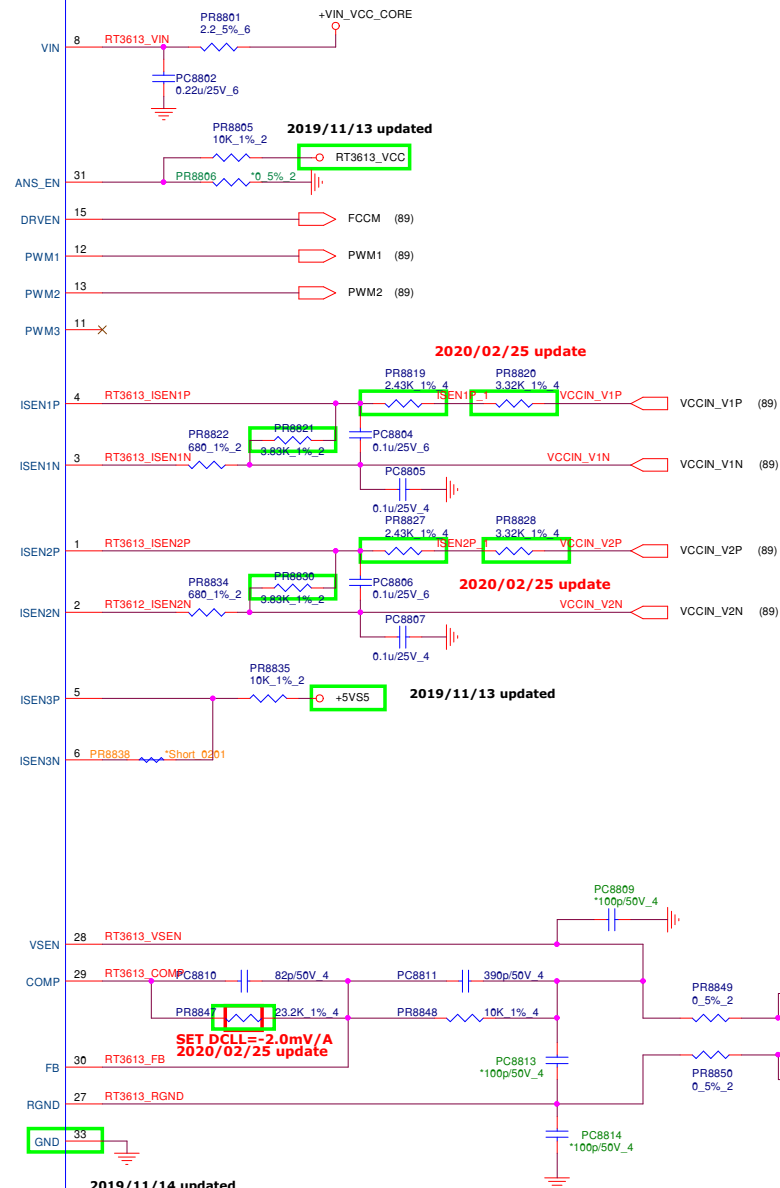
Size Custom	Document Number 98 -- reserve page(N.A)	Rev 1A
Date: Friday, August 21, 2020		Sheet 84 of 106

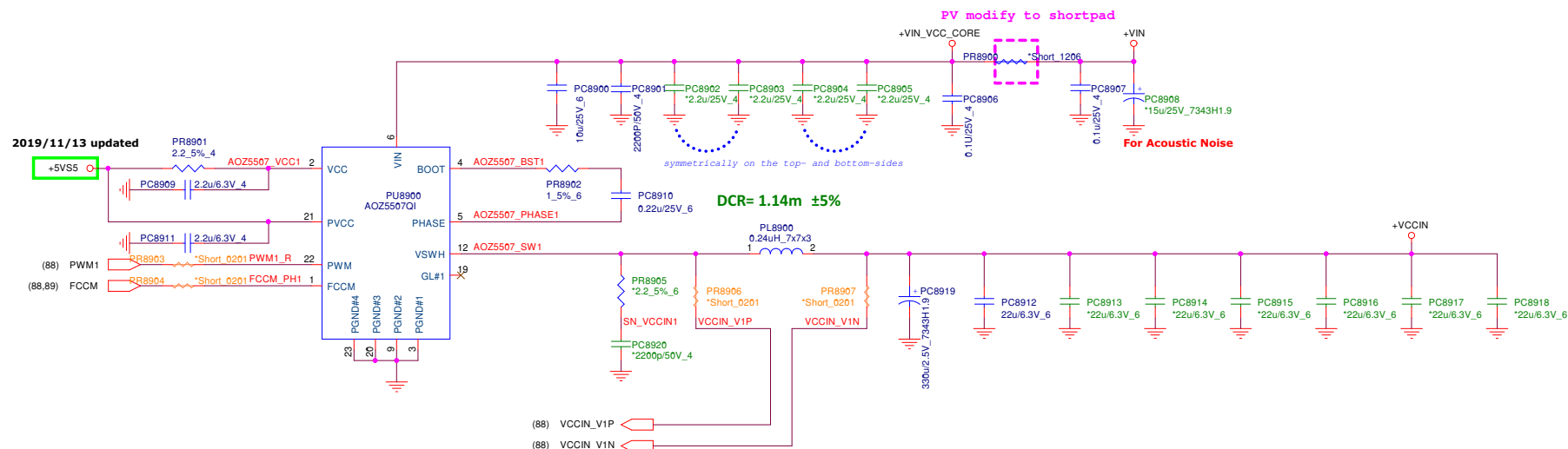
(5,10,12,15,16,19,35,41,47,63,66,78,91,93,95,96,105) +3VS5
 (10,14,15,16,19,41,54,61,63,64,78,81) +3VPCU
 (15,19,57,61,76,87,88,89,91,93,96,98,102,105) +5VS5
 (41,81,95,96,105) +5VPCU
 (18,20,34,50,78,82,87,89,91,97,98,102) +VIN



USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff



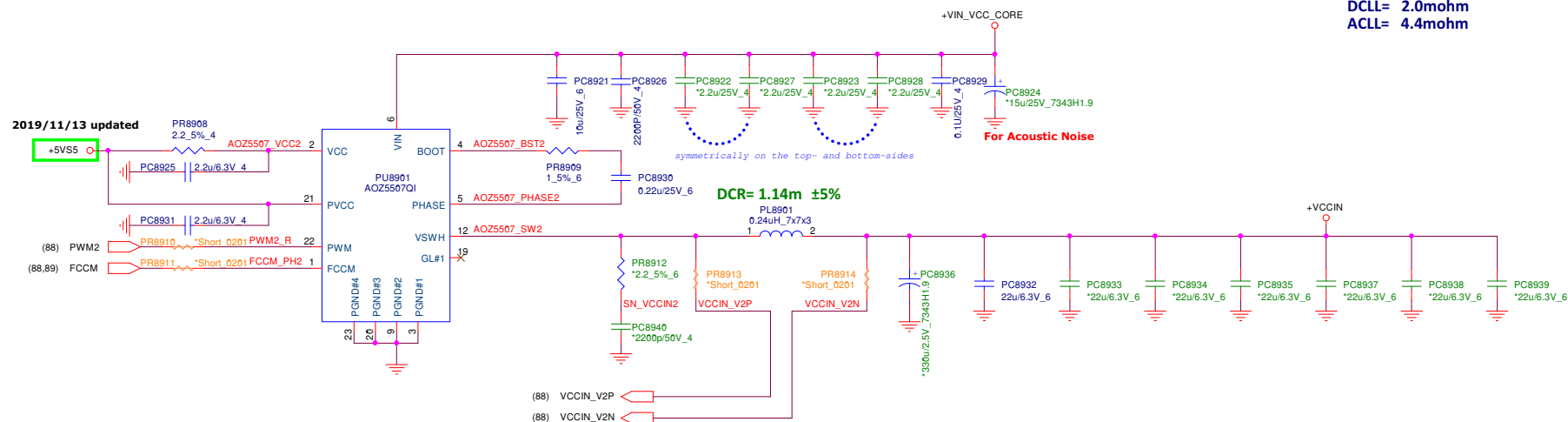





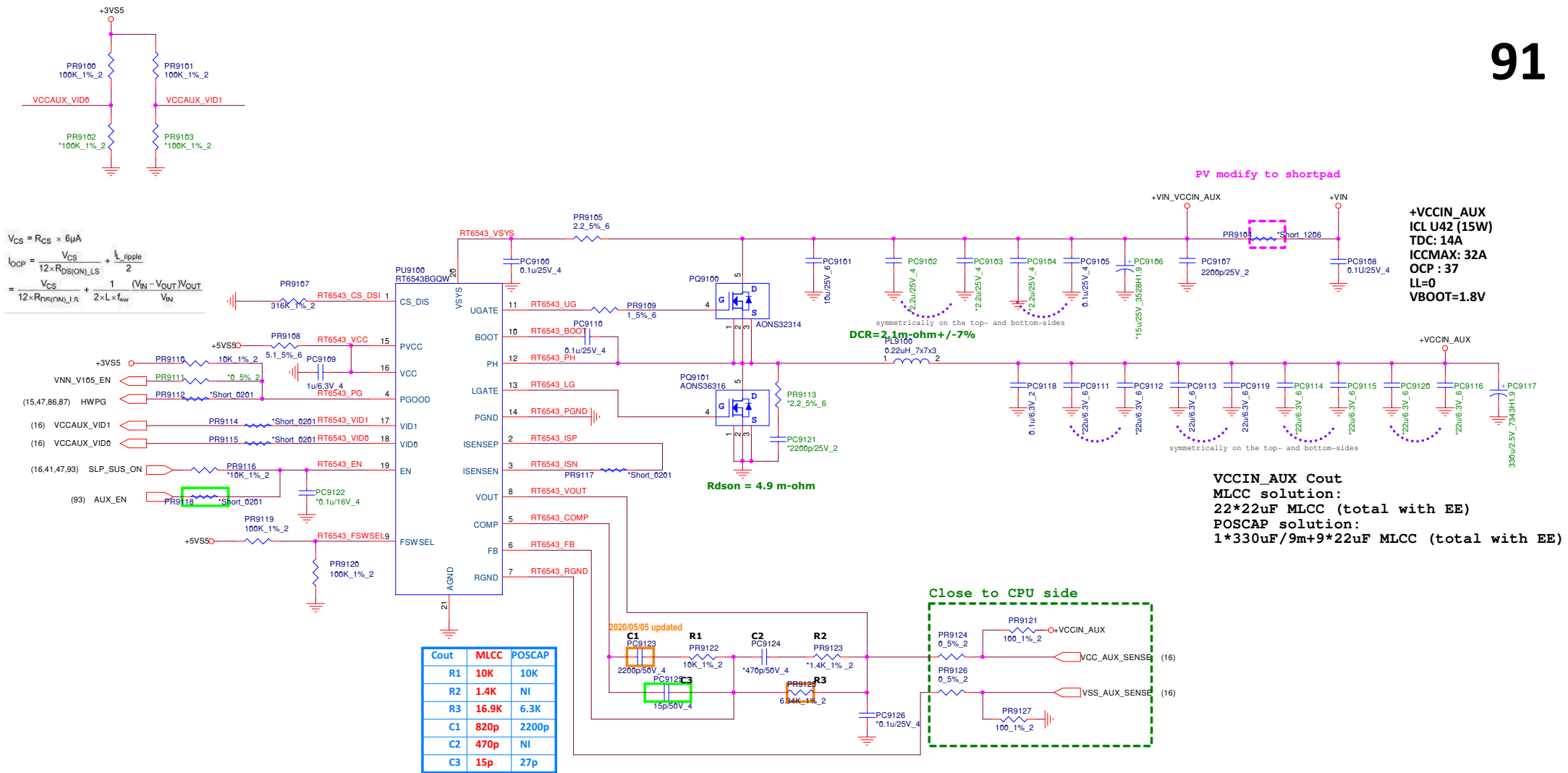
IMVP9 Design: TGL UP3 4+2 (15W)_Performance line
2-phase, Inductor DCR Sensing

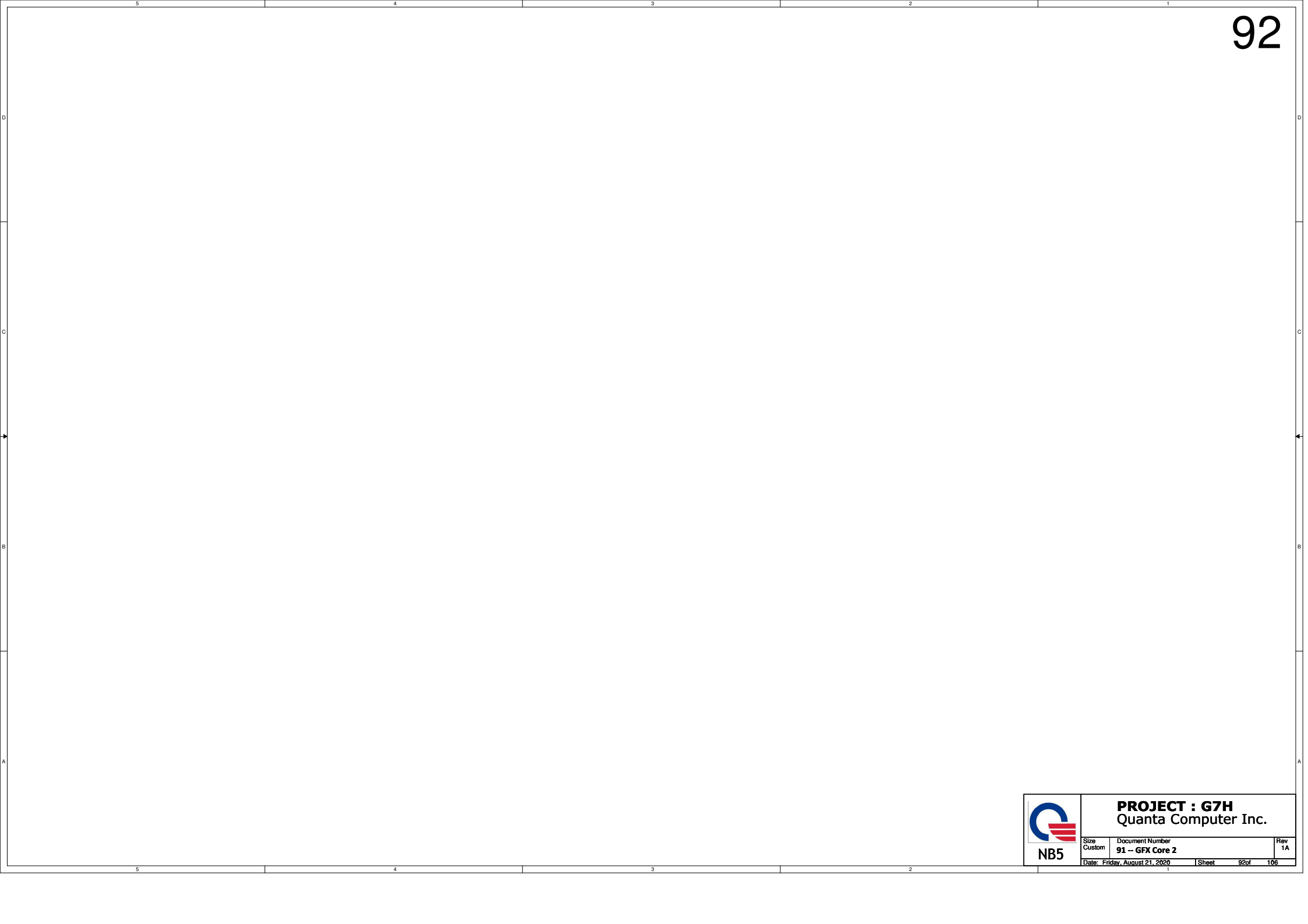
Ref DOC#: 607872 & 575683


VCCIN rail
Vboot=0V
TDC=36A
Iccmax=55A
Iccmax Transient=65A (10mS)
OCP(min)=75A
DCLL= 2.0mohm
ACLL= 4.4mohm



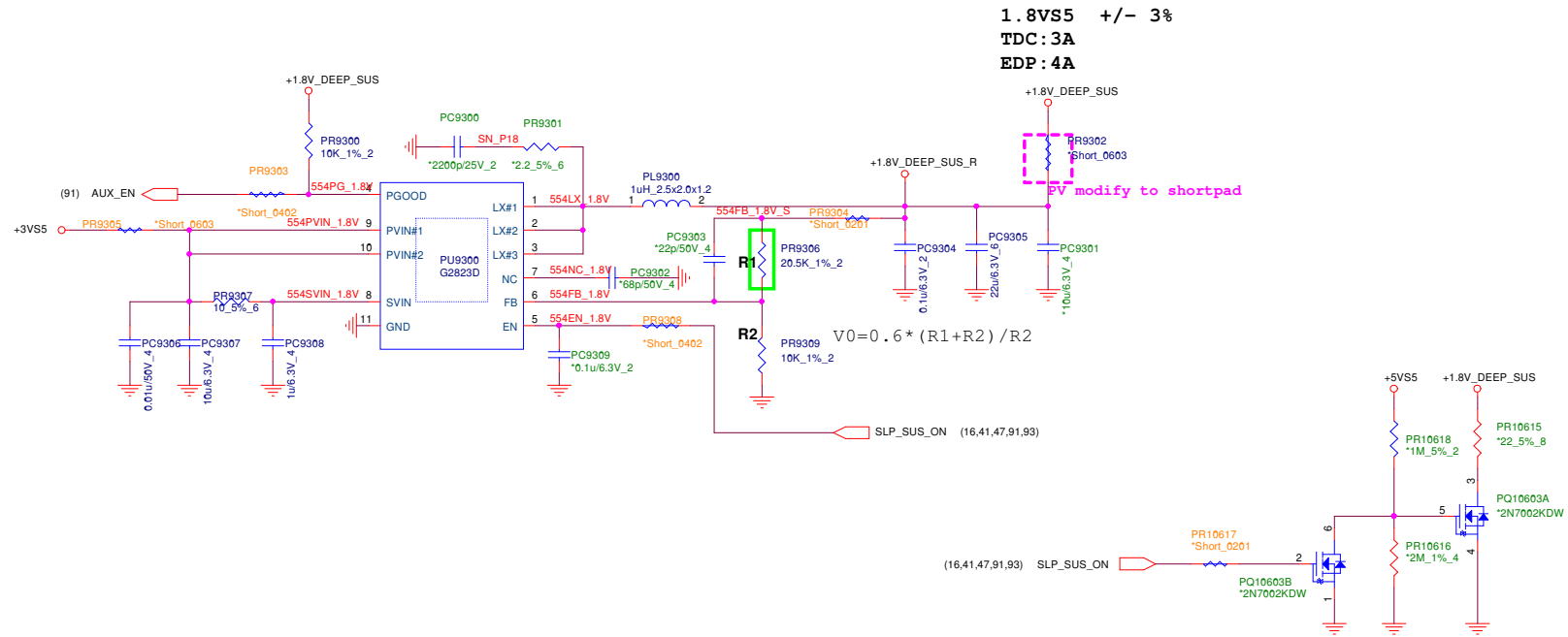
	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number 91 -- GFX Core 2	Rev 1A
	Date: Friday, August 21, 2020		Sheet 90 of 106





 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number 91 -- GFX Core 2	Rev 1A
	Date: Friday, August 21, 2020		Sheet 92 of 106


+VIN (18,20,34,50,78,82,86,87,89,91,97,98,102)
 +3VS5 (5,10,12,15,16,19,35,41,47,63,66,78,86,91,95,9,105)
 +5VS5 (15,19,57,61,76,86,87,88,89,91,96,98,102,105)
 +1.8V_DEEP_SUS (10,12,14,16,18,41,47,76,78,96,105)
 MAINON (41,47,87,95,96)

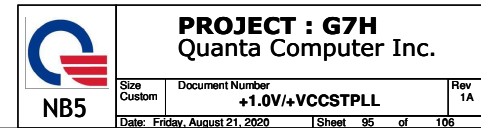


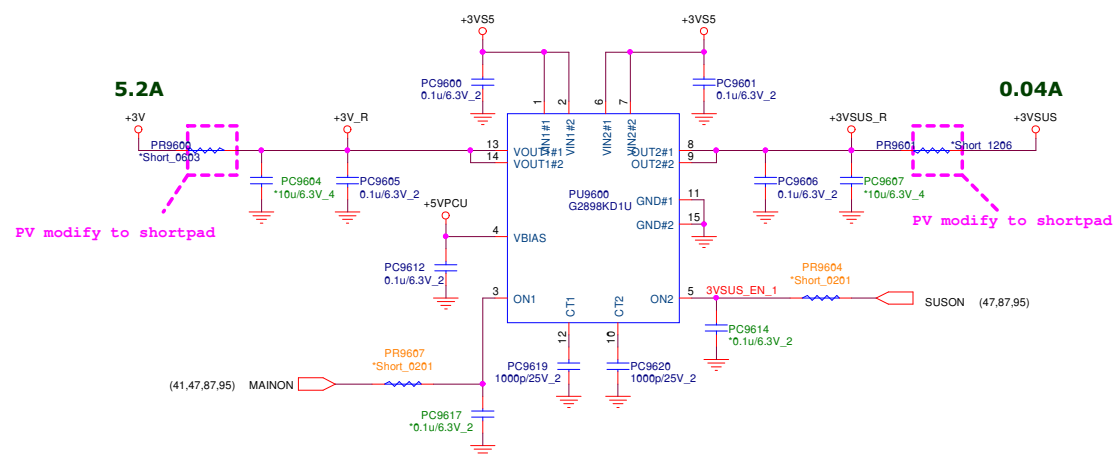
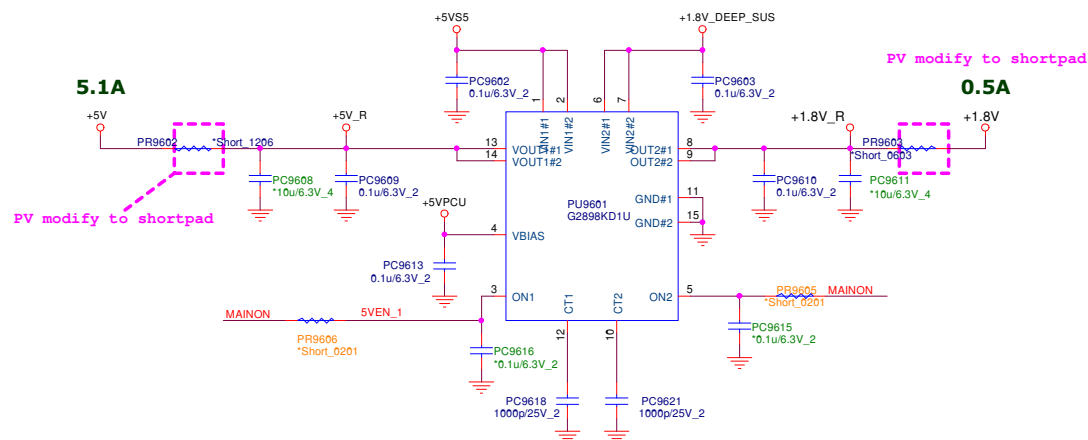
PROJECT : G7H
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+1.8V_DEEP_SUS	1A
Date: Friday, August 21, 2020	Sheet 93 of 106	

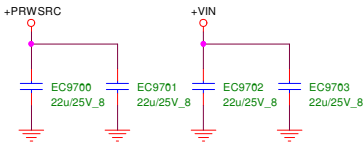
NB5

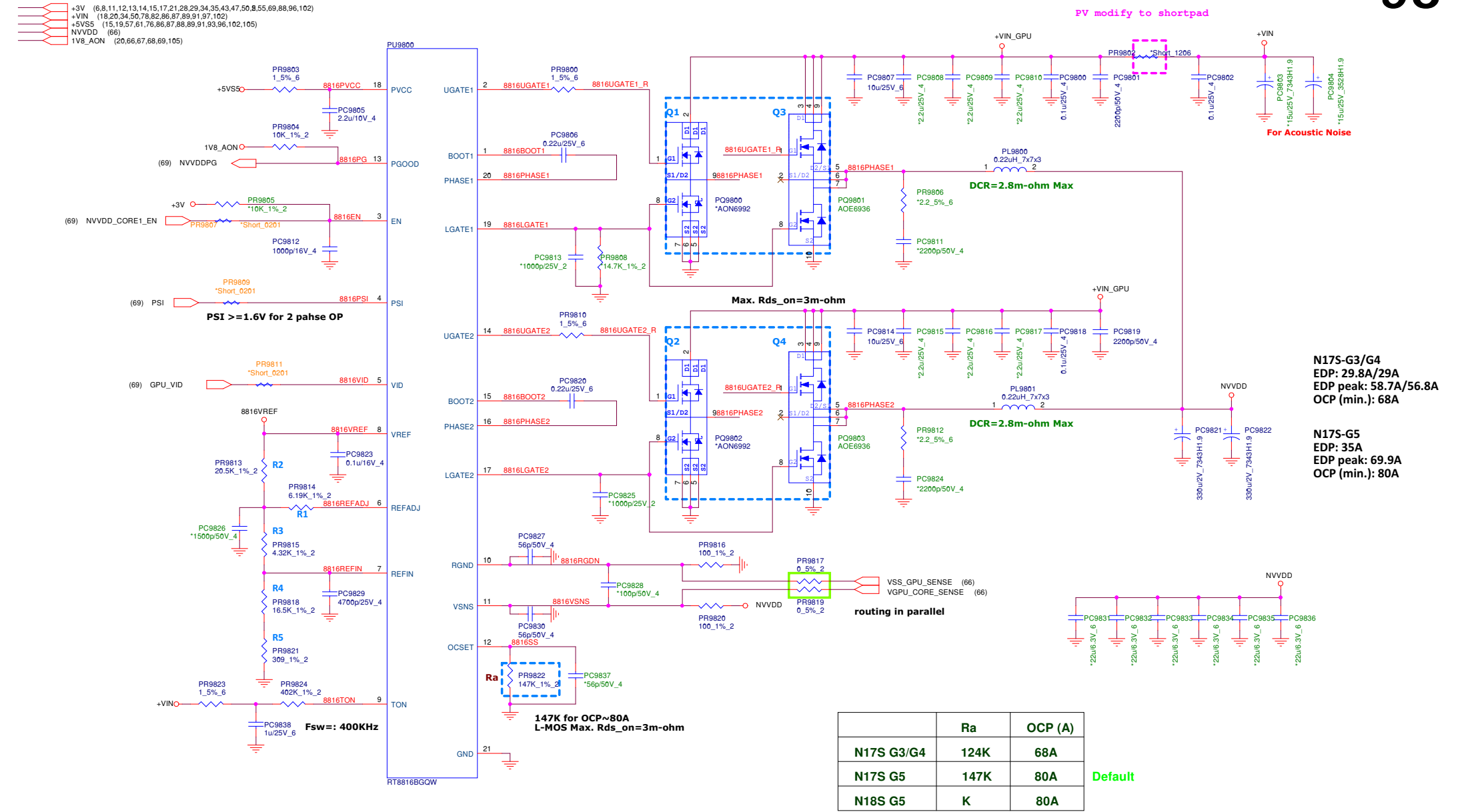
 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number 99 -- reserve page	Rev 1A
	Date: Friday, August 21, 2020		
Sheet		94 of	106





Reserve for ISEN






N17S-G3/G4
EDP: 29.8A/29A
EDP peak: 58.7A/56.8A
OCP (min.): 68A

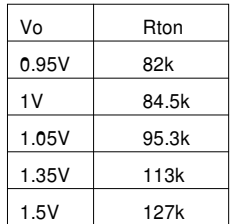
N17S-G5
EDP: 35A
EDP peak: 69.9A
OCP (min.): 80A



PROJECT : G7H
Quanta Computer Inc.


Size Custom	Document Number A0 – reserve page	Rev 1A
Date: Friday, August 21, 2020		
Sheet 100 of 106		


	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number A1 – reserve page	Rev 1A
	Date: Friday, August 21, 2020 Sheet 101 of 106		



	1.35V	Control
N17S G3/G4	5.8A	G5335A
N17S G5	7.1A	G5335

Default

 NB5	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number A3 -- reserve page	Rev 1A
	Date: Friday, August 21, 2020 Sheet 103 of 106		

	PROJECT : G7H Quanta Computer Inc.		
	Size Custom	Document Number A2 – reserve page	Rev 1A
	Date: Friday, August 21, 2020 Sheet 104 of 106		

+3VS5	(5,10,12,15,16,19,35,41,47,63,66,78,86,91,93,99)
+5VS5	(15,19,57,61,76,86,87,88,89,91,93,96,98,102)
1V8_MAIN	(20,66,67,68)
1V8_AON	(20,66,67,68,69,98)
+1.2VSUS	(5,7,9,18,28,29,87)
PEX_VDD	(20,66,68)
MAINON	(41,47,87,95,96)

